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PACIFIC: the readout ASIC for the SciFi Tracker of the upgraded LHCb detector

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Abstract: The LHCb detector will be upgraded during the Long Shutdown 2 (LS2) of the LHC in order to cope with higher instantaneous luminosities and will switch to a 40 MHz readout rate using a trigger-less software based system. All front-end electronics will be replaced and several sub-detectors must be redesigned to cope with the higher detector occupancy and radiation damage. The current tracking detectors downstream of the LHCb dipole magnet will be replaced by the Scintillating Fibre (SciFi) Tracker. The SciFi Tracker will use scintillating fibres read out by Silicon Photomultipliers (SiPMs). State-of-the-art multi-channel SiPM arrays are being developed and a custom ASIC, called the low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC), will be used to digitise the signals from the SiPMs.

This article presents an overview of the R&D for the PACIFIC. It is a 64-channel ASIC implemented in 130 nm CMOS technology, aiming at a radiation tolerant design with a power consumption below 10 mW per channel. It interfaces directly with the SiPM anode through a current mode input, and provides a configurable non-linear 2-bit per channel digital output. The SiPM signal is acquired by a current conveyor and processed with a fast shaper and a gated integrator. The digitization is performed using a three threshold non-linear flash ADC operating at 40 MHz. Simulation and test results show the PACIFIC chip prototypes functioning well.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Digital electronic circuits

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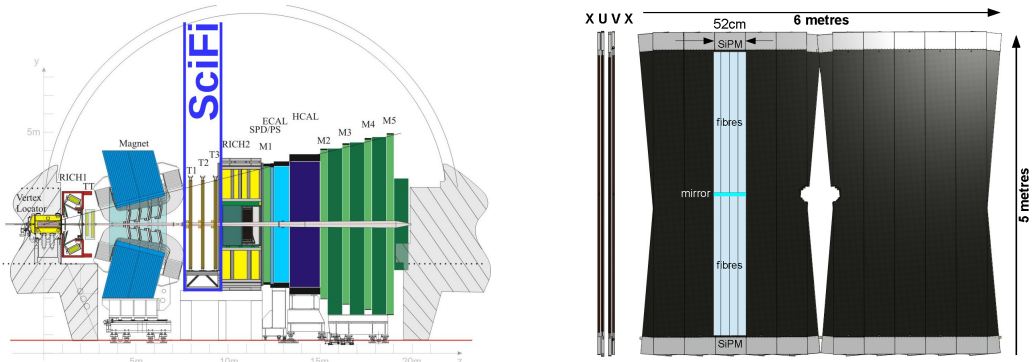
1 LHCb and the SciFi Tracker

The LHCb detector, shown in figure 1a, is a single-arm forward spectrometer at CERN designed for studying particles containing b or c quarks and indirectly searching for New Physics. A full description of the LHCb detector can be found in ref. [1]. The measurements to date have not shown any significant deviations from the Standard Model not accounted for by statistical experimental uncertainties. In order to overcome this, an upgrade of the LHCb detector is planned to increase the total integrated luminosity from the current $3\,\text{fb}^{-1}$ after 2012 to $50\,\text{fb}^{-1}$ over 10 years with a more efficient selection of events [2, 3].

To achieve this, the current 1 MHz hardware trigger will be replaced by a 40 MHz software trigger at the front-end (FE) electronics level. Moreover, the upgraded detector will be operated at an increased instantaneous luminosity of $2{\cdot}10^{33}$ $\text{cm}^{-2}\text{s}^{-1}$. This increase in luminosity has a significant impact on the tracking detectors downstream from the magnet, indicated in figure 1a. The increased detector occupancy and ionising radiation near the beam pipe are too large for the currently installed detector system.

As a replacement for the downstream tracking detectors, the Scintillating Fibre (SciFi) Tracker [4] is being developed. The SciFi Tracker will use plastic scintillating fibres with a diameter of 250 μm as the active material which also transports the optical signal to the photodetectors. The fibres have an attenuation length of about 3.5 m, a propagation speed of 6 ns/m, and a scintillation decay time of 2.8 ns. The fibres are wound into 2.5 m long six layer mats and mirrored at the inner end to improve the light yield. The scintillating light is collected by 128-channel arrays of pixelated silicon photomultipliers (SiPM) with a pitch of 250 μm. These sensors provide a photon detection efficiency above 40% and a gain larger than 10^6 e^-/PE in a highly compact design. The SciFi Tracker is composed of three stations, placed along the beam at the same positions as the current Outer Tracker. One station consists of four planes, each covering a $5 \times 6\ \text{m}^2$ area. The two



(a) Side view [4].

(b) Layout of a SciFi tracking station [5].

Figure 1. The LHCb detector.

internal planes are tilted at a stereo angle of ±5°with respect to the two external vertical planes, as displayed in figure 1b. The planes are further divided into 10-12 independent modules with readout boxes (ROB) at the top and the bottom. Each module is populated with eight fibre mats, while a ROB encloses 16 SiPM arrays and the corresponding FE electronics needed for the signal acquisition. In total, this amounts to over 580k SiPM channels, allowing for a position resolution below 100 μm in the horizontal plane.

1.1 Front-end electronics

The front-end (FE) electronics provide the back-end with a digital representation of the position of the detected particles. For this purpose, the modular system shown in figure 2a was developed, which is comprised of three elements: the analog board, the clusterization board and the master board. The analog board contains the ASIC chip, the PACIFIC, described in detail below, which acquires, processes and digitises the analog SiPM signals. The PACIFIC creates a 2-bit signal for each channel indicating which of three amplitude thresholds have been exceeded. From the digital output of the analog board, the clusterization board FPGA performs additional processing of the PACIFIC output. It computes the barycenter for each cluster of signals produced by a particle track, improving the resolution intrinsic to the geometrical layout of the sensors. Additionally, this processing serves as a zero suppression mechanism, greatly reducing the required throughput. The clustering process also serves to suppress noise from thermally generated low-amplitude signals in the SiPM. The master board collects the data from the clusterization boards and send it through a fast communication link using the GBT chipset [6] and Versatile Link [7] devices. Furthermore, this board is equipped with DC/DC converters [8] to power the whole FE.

2 PACIFIC

The low-Power ASIC for the sCIntillating FIbres traCker (PACIFIC) is a 64-channel ASIC implemented in 130 nm CMOS technology, aiming at a radiation tolerant design with a power consumption below 10 mW per channel. It is foreseen to connect the PACIFIC directly to the SiPM with no additional components, demanding a current mode input. The analog processing must assure an operation with no dead time and a negligible level of spillover. The 15 ns spread in the time of

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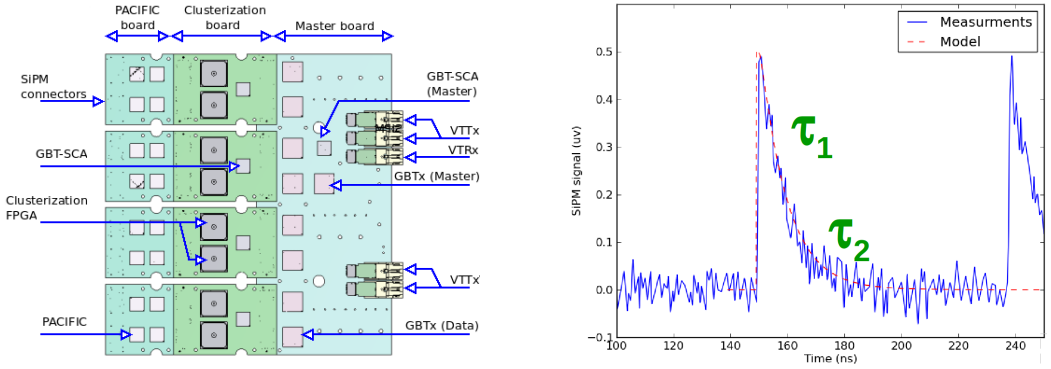


(a) Schematic of the FE boards.

(b) SiPM pulse shape.

Figure 2. The FE electronics of SciFi.

arrival of the signal due to the length of the scintillating fibres has a significant impact on this signal processing. Moreover, the pulse shape generated by the SiPM, modelled as the double exponential decay represented in figure 2b, yields a recovery time around 50 ns, requiring the fast shaping stage.

The architecture implemented in each PACIFIC channel is presented in figure 3. The input stage is a current preamplifier with low input impedance. It also fixes the voltage at the input node, tunable over a 700 mV range, thus allowing a correction of the SiPM bias voltage. Additionally, this stage has four selectable gains to handle various dynamic ranges. The following stage is a fast shaper, with a fully configurable double pole-zero cancellation. It grants the cancellation of the SiPM long tail, reducing the full width at half maximum (FWHM) of the produced pulse below 5 ns. The last analog stage is a dual interleaved gated integrator, switching every 25 ns between its two units. The signal is then digitized as 2-bits with a non-linear flash ADC with three configurable thresholds that correspond to the ones defined in an optimized clusterization algorithm. Finally, the output from two channels is encoded in four bits and serialized at 160 MHz.

The target power consumption is low, below 600 mW, therefore the lowest available voltage supplies were selected, 1.2 V for the core and 1.5 V for the pad ring. The PACIFIC is equipped with fully tunable common biasing circuitry and an I^2C slave for the management of the configuration registers.

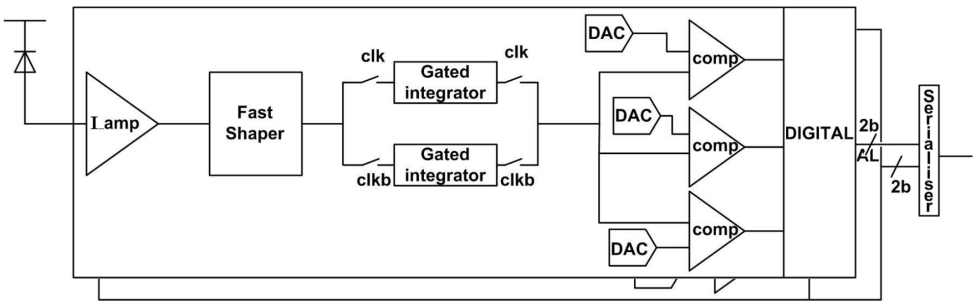


Figure 3. PACIFIC channel architecture [9].

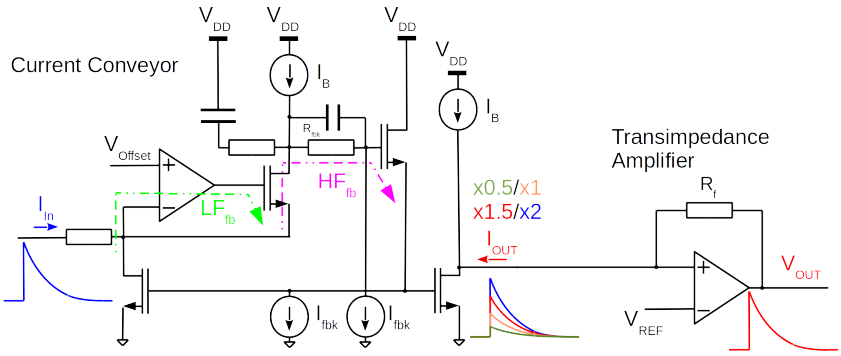


Figure 4. Schematic of the input stage [4].

2.1 Input stage

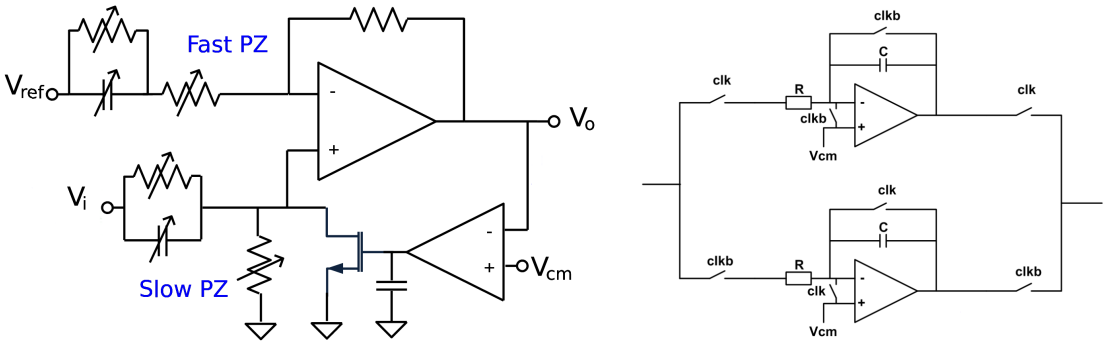
The input stage is a low voltage current mode preamplifier designed to sink current from the anode of a SiPM. To avoid interfering with the signal shape of the sensor, this stage has a target bandwidth higher than 250 MHz. Up to this frequency, it must consistently present an impedance of $\approx 50\ \Omega$ at the input node while assuring a constant DC level at this same node. It is composed of a current conveyor followed by a transimpedance amplifier, as depicted by the schematic of figure 4.

The current conveyor employs a novel approach with a double feedback. The low frequency feedback (LF_{fb}), based on a low input-impedance current amplifier [10–12], sets the offset voltage at the input node through the virtual short circuit of a folded cascode operational transconductance amplifier (OTA). This OTA drives a follower in a low frequency range and thus closing the LF_{fb} loop. The high frequency feedback loop (HF_{fb}) employs a common-gate regulated cascode configuration [13] in order to keep low input impedance constant at signal bandwidth. Several selectable slave branches are implemented in the output mirror to produce the different gains.

The current conveyor is followed by a closed-loop transimpedance amplifier where the SiPM current signal is converted into a voltage signal for further processing and the output voltage is controlled to keep linearity. For this purpose, a high speed OTA is employed with a GBW larger than 250 MHz, a high sourcing current capability and a low power consumption (700 μW).

2.2 Shaping stage

The shaping stage relies on the pole-zero cancellation technique to reduce the width of the SiPM pulse to fit the 10 ns left by the time of arrival spread within the clock period, thus minimizing spillover and the fluctuation introduced by the arrival time on the integrated signal. It is implemented using an OTA based close loop configuration with a passive cancellation net on each input, as illustrated in figure 5a. The net on the non-inverting input suppresses the slower time constant of the SiPM response, related to its internal capacitance and the quenching resistor. On the other hand, the net on the inverting branch takes on the faster time constant, related to parasitic interconnect capacitance and the load applied to the sensor. The different components of both nets are tunable, allowing to control the undershoot as well as the pulse width. Lastly, an active DC feedback loop is used to control the quiescent output voltage prior to the integration.



(a) Fast pole-zero cancellation shaper [4].

(b) Dual gated integrator [4].

Figure 5. Schematics of the analog processing stages.

2.3 Integration stage

The integration stage is included at the end of the analog processing to average the photo-statistical fluctuations before digitization. The process is performed with gated integrators using the classical architecture and based on a Miller OTA with a GBW of 200 MHz and 300 μW of power consumption. Two complementary units are interleaved, as shown in figure 5b, and alternatively activated and reset at a 20 MHz rate. This way one is integrating while the other resets, allowing to extend the integration window over the whole 25 ns clock period and thus avoiding any dead time during the acquisition. The offset at the output of each integrator can be adjusted with an open-loop current-injection circuit, based on a resistor and a series of DAC controlled current mirrors. This addition allows to correct the potential mismatch between the DC level of the two units due to the fabrication process.

2.4 Digitization stage

The digitization stage has been designed to fit the needs of the clusterization processes that follows. Three configurable thresholds define the transitions between the values of the two-bit non-linear flash ADC employed. The thresholds are derived from the channel DC reference using current DACs, assuring the coherence among all these voltage levels. Each threshold is confronted every 25 ns to the channel signal in a dedicated comparator with a hysteresis of 10 mV and ranging from the DC reference down to 20 mV. The channel signal is provided by a dual track and hold operating synchronously with the integration stage. Two Miller track and holds [14] alternatively sample each integrator, merging their signals at the output. Since the thresholds and reference voltage are shared throughout the chip, a closed-loop DC correction is included at this point to assure the required homogeneity in the offset of the different channels before the comparators.

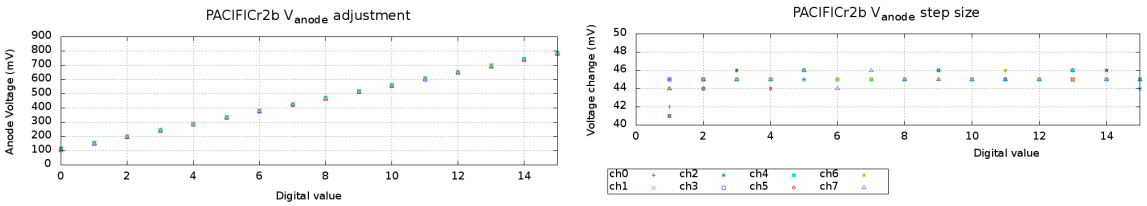
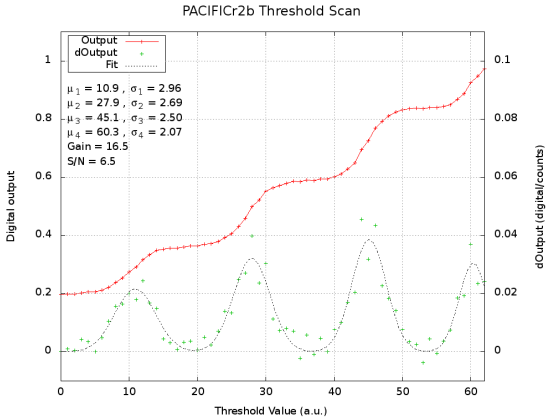


Figure 6. Input voltage control sweep.



(a) Gain extraction from threshold scan.

	@3V OverVoltage		@3V5 OverVoltage	
Ch	**Gain**	**Variation %**	**Gain**	**Variation %**
0	16.5	0.2	18.9	-1.8
1	15.6	-5.3	19.2	-0.2
2	16.1	-2.3	18.2	-5.5
3	15.8	-4.1	18.3	-4.9
4	17.2	4.4	20.3	5.5
5	17.4	5.6	20.6	7
6	17.4	5.6	20.3	5.5
7	15.8	-4.1	18.2	-4.9
μ	16.48		19.25	

(b) Gain spread at two SiPM overvoltages.

Figure 7. Gain measurement of PACIFICr2 connected to a Hamamatsu SiPM array.

3 Prototypes

The PACIFICr2 chip was the first prototype to include the whole processing chain, including the digitization stage and internal biasing circuitry. Three units have been mounted on a two-board setup for testing. The devices have an average power consumption of 6.42 mW per channel, well within specifications. Figure 6 presents the response of the voltage control at the input node of the channel. The DAC covers the expected range, between 100 mV and 800 mV, with a reasonable linearity. The output of the analog stages has been examined through the dedicated debug outputs. An average of 32 measurements is shown in 9a, where the preamplifier and shaper signals were acquired without a clock to avoid adding switching noise.

Once the correct operation of the individual channels has been validated, the test setup is expanded by connecting a Hamamatsu SiPM array and exciting it with a blue picosecond pulsed laser diode. The photopeak bands observed in the SiPM analog output can be observed in the PACIFIC digital output by scanning the threshold setting of the comparators, and counting the number of events that exceed threshold, as seen in in figure 7a. The curve (red) clearly exhibits the expected step function representing the individual photoelectrons, ascertaining the single photoelectron resolution of the channel architecture. Taking the derivative of this response (grey), the gain of the system can be calculated as the difference between two consecutive peak structures. Table 7b details the gain measurements of the different channels of one chip, presenting a variation only slightly higher than the 10% reported by the SiPM manufacturer. However, the threshold scan curves of these channels are shifted more widely, as displayed in figure 8a. This effect is produced by the offset variation among the channels in the PACIFIC, accounting for ≈1 PE. Additionally, the offset mismatch between the two integrators within a single channel can also reach ≈1 PE, as depicted in figure 8b. Both offset variation measurements were corroborated afterwards with Monte Carlo simulations. Since the threshold levels are shared by all the channels, the offset variations hinder the tracking capabilities of the PACIFICr2 version of the chip.

A new version of the chip has already been manufactured. PACIFICr3 is the first full 64 channel prototype, aiming at complete functionality for physics measurements. The design has

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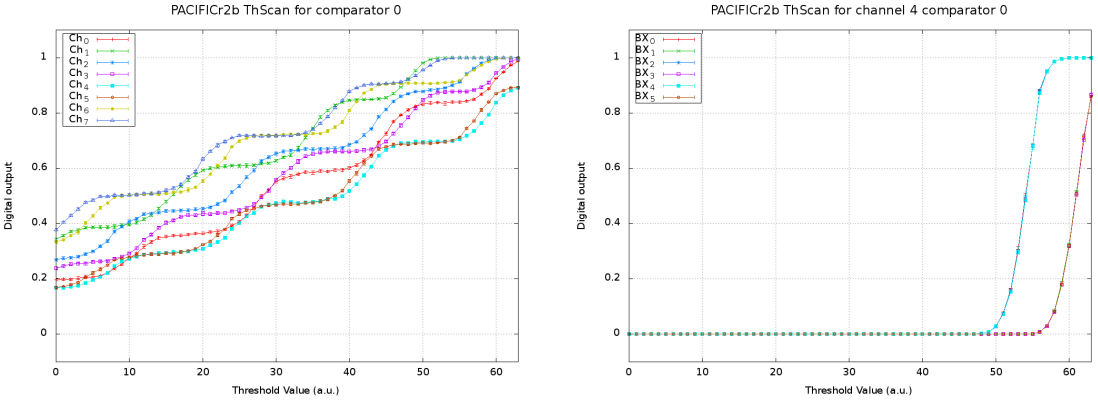
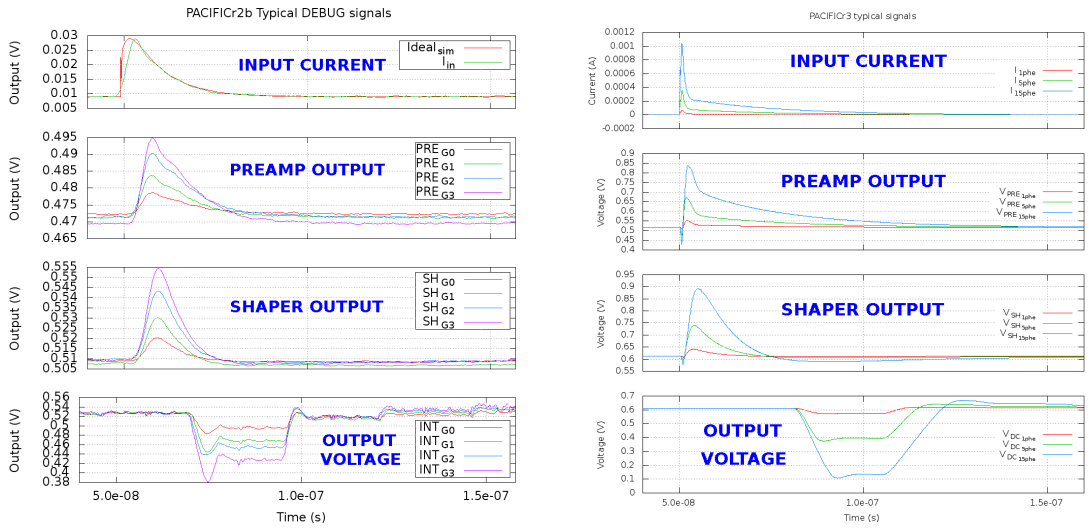


(a) Spread among channels in a single device.

(b) Worst case mismatch between integrators.

Figure 8. Effects of the offset variation on the digital output.

been migrated from IBM to TSMC 130 nm technology, requiring a new layout and development. The channel pitch on the chip was increased to 80 μm, yielding a new floor-plan with double-sided inputs and a symmetrical arrangement. Regarding the processing channel, the shaper was reconfigured according to the response of the latest SiPM prototypes. This version also includes the offset correction mechanisms described in sections 2.3 and 2.4 to counteract the effects observed in the previous prototype. According to detailed simulation, the analog response is expected to remain close to PACIFICr2, as shown in figure 9.



(a) PACIFICr2 measured with different gains.

(b) PACIFICr3 simulated with different input level.

Figure 9. Signal output at the different analog stages.

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4 Conclusion and outlook

The PACIFIC is an ASIC designed for fast scintillating fibre trackers read out by SiPMs at particle accelerators like the LHC. It provides fast shaping time, with low spillover due to the pole-zero cancellation shaper that suppresses the long time constant related to SiPM recovery time. Moreover, it assures an operation with no dead-time thanks to the dual gated integrator. Furthermore, the preamplifier and the shaper can be tuned to adapt to production variations and different operating points. The second PACIFIC prototype has fully validated the channel architecture, presenting a behaviour fully adapted to the goals of this chip. A third prototype has been manufactured including mechanisms to correct the integration issues observed in previous prototypes. The test of this third version of the chip with a detailed performance analysis remains as future work.

Acknowledgments

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