

# Reconfigurable ASIC for a low level trigger system in Cherenkov Telescope Cameras

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## Reconfigurable ASIC for a low level trigger system in Cherenkov Telescope Cameras

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**ABSTRACT:** A versatile and reconfigurable ASIC is presented, which implements two different concepts of low level trigger (L0) for Cherenkov telescopes: the Majority trigger (sum of discriminated inputs) and the Sum trigger concept (analogue clipped sum of inputs). Up to 7 input signals can be processed following one or both of the previous trigger concepts. Each differential pair output of the discriminator is also available as a LVDS output. Differential circuitry using local feedback allows the ASIC to achieve high speed (500 MHz) while maintaining good linearity in a 1 Vpp range. Experimental results are presented. A number of prototype camera designs of the Cherenkov Telescope Array (CTA) project will use this ASIC.

**KEYWORDS:** Analogue electronic circuits; Trigger concepts and systems (hardware and software); Trigger detectors; VLSI circuits

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## 1 Introduction

Cherenkov telescopes are used to detect Very High Energy (VHE,  $E > 10$  GeV) gamma rays after their interaction with the Earth's atmosphere ([1–3] and [4]). By detecting and processing Cherenkov light produced by gamma-ray-induced Extensive Air Showers (EASs) composed of relativistic electrons and positrons, it is possible to characterize the incoming gamma ray in terms of direction and energy. Placing several telescopes (of different sizes) together to observe the same shower in coincidence results in a gamma-ray detector with enhanced sensitivity over a wide energy spectrum.

Cameras based on fast and sensitive photo-sensors, typically photomultiplier tubes (PMTs), detect Cherenkov light. An electronic readout chain coupled to each photo-sensor digitizes the PMT waveform. The readout chain also incorporates an electronic trigger chain that performs fast signal processing. Rapid signal processing is necessary for disentangling signals produced by incident Cherenkov light from EASs from those induced by background light from the night sky background (NSB).

In this paper, an Application Specific Integrated Circuit (ASIC) designed specifically for the lower level camera trigger decision in Cherenkov telescopes is presented. The ASIC can be configured to perform two different analogue triggering schemes, which we call majority and sum triggering. It also provides an interface for digital trigger systems.

There are a number of motives for implementing multiple trigger schemes in the same chip. First, the majority trigger scheme is a simple and robust system, traditionally implemented in Cherenkov telescopes. In contrast, the sum trigger involves a novel concept (described in section 2.1), first implemented in the MAGIC telescopes [5], which aims to reduce Cherenkov telescopes'

energy threshold as much as possible. Second, it will be very useful for telescope to have the ability to choose between the two triggering systems depending on different observing conditions. Observing conditions may change as the telescopes are pointed to different regions of the sky with varying NSB levels. In addition, different types of telescopes in CTA can use the same ASIC to implement different trigger schemes. Large Size Telescopes (LSTs), which incorporate 23 m diameter reflectors to study the low energy regime, will need to use the sum trigger scheme when observing weak point sources with high-energy spectra that peak at lower energies. Medium Size Telescopes (MSTs) might choose the majority trigger for its more robust operation.

Finally, the discriminated output of the individual pixels in low-voltage differential signalling (LVDS) format allows telescopes to implement a digital trigger system, in which the discriminated outputs of all the pixels in the camera can be combined to search for complex patterns. In this way, images from muons or even hadrons could be identified at the trigger level.

Section 2 describes a typical multilevel trigger approach used for Cherenkov telescope cameras [6]. Section 3 presents the architecture of a new versatile ASIC for the implementation of the low level trigger. Section 4 includes measurements of functionality and performance of the ASIC. Conclusions are given in section 5.

## 2 Trigger architecture

### 2.1 Trigger concept

The trigger decision in Cherenkov telescopes is based on the detection of a concentration of signal in the camera both in space and time. The photons coming from a Cherenkov shower will be detected by several close pixels in a time window of a few nanoseconds. Therefore, a telescope trigger, requiring a given number of pixels of the camera with a minimum number of photons in a short time, will reject a sizeable amount of NSB-induced events because NSB photons are not correlated either in space or in time.

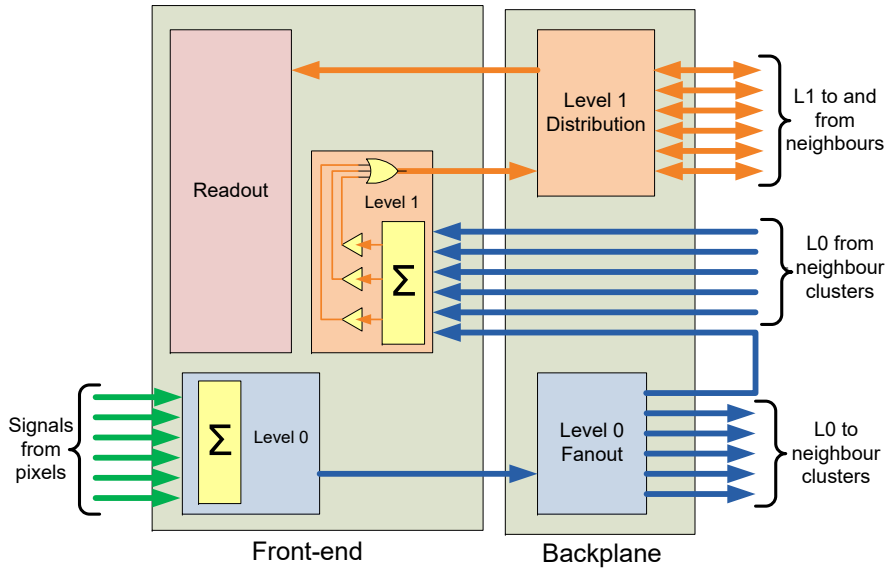
Two different strategies for triggering are typically used in Cherenkov telescopes based on fast digitizers [6]. A majority trigger architecture consists of the discrimination of the signals coming from pixels, in order to count the number of activated pixels in a region. After discrimination, the signal processing can be analogue or digital. The sum trigger strategy is to sum the pulses from the pixels in a region and compare them with a threshold defined for the entire region. In a multilevel trigger architecture, these two strategies can both be implemented in the lower level (L0) trigger, while the higher level (L1) trigger circuit remains the same.

Our trigger system is designed for cameras made up of 7-pixel modules. One module consists of PMTs, front-end circuits, digitization and readout electronics, and trigger decision and distribution electronics.

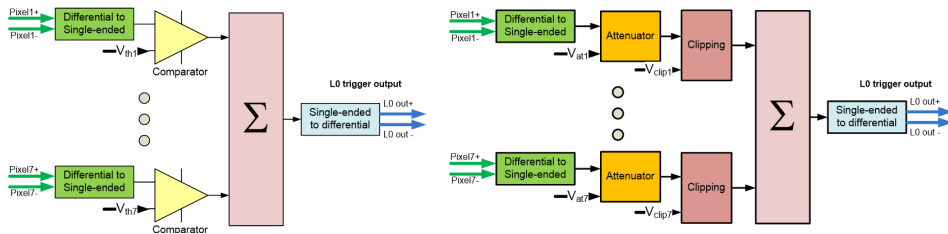
### 2.2 Architecture of the trigger

The signal from every pixel is amplified and feeds a fast readout digitizer like the NECTAr [7] or DRAGON [8] readout boards. A two-level trigger scheme has been developed that is compatible with the electrical and mechanical architecture of some of the telescopes' cameras proposed for CTA. This scheme is shown in figure 1.

The first level, which we call L0, is module-based and combines the signals of the pixels in each module. In this level, the trigger implements the majority and sum trigger strategies, as shown



**Figure 1.** Block diagram of the two-level analogue trigger.



**Figure 2.** Simplified block diagrams of the L0 trigger illustrating the majority (left) and sum (right) triggering schemes.

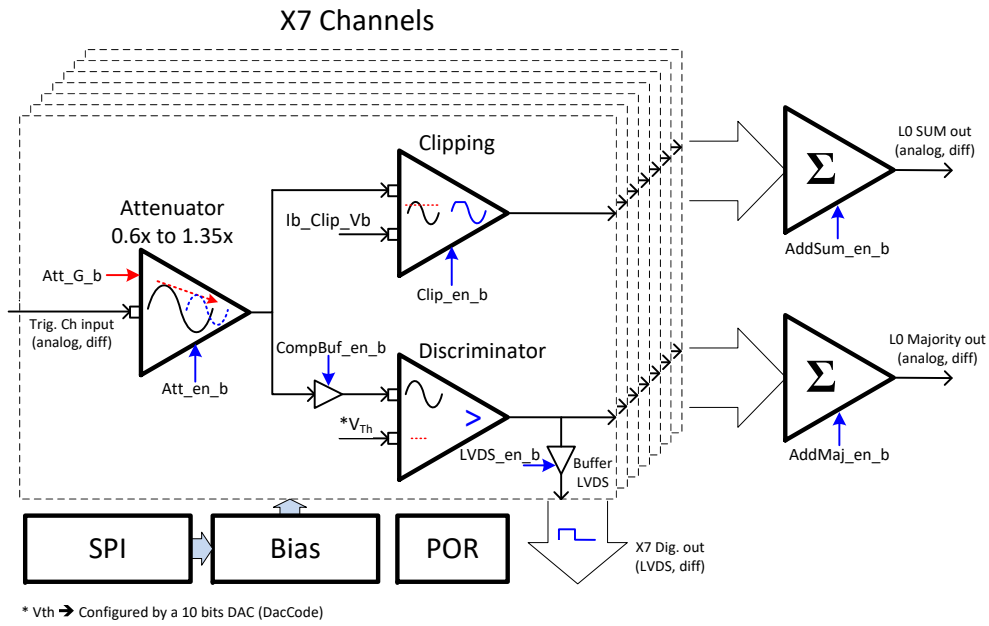
in figure 2. The sum trigger performs an analogue sum of the signals from all pixels in the module. Before adding the signals from the individual pixels, each of them goes through attenuator and clipping circuits (both slow-control adjustable). The former allows all pixel gains to be equalized with a precision better than 5%. The latter clips the signals greater than a given value, which limits the influence of after-pulses from the photosensors. A detailed description of the ASIC implementing the L0 subsystem is presented in section 3.

The second level, called L1, is also implemented in each module and combines the L0 signals of neighbouring modules from specific trigger regions with the local L0 signal. The L1 will generate a digital trigger pulse, which is distributed to the digitizers of all modules in the camera and is the final camera trigger. Another ASIC implements the L1 trigger level [10].

### 3 ASIC design

Our mixed signal ASIC is designed to implement several low-level trigger functionalities. A block diagram is shown in figure 3.

Both majority and sum trigger analogue schemes are implemented. The output of each majority discriminator is externally accessible, so a simple majority decision or a high-level trigger scheme can be implemented in a programmable logic device (typically an FPGA or CPLD).



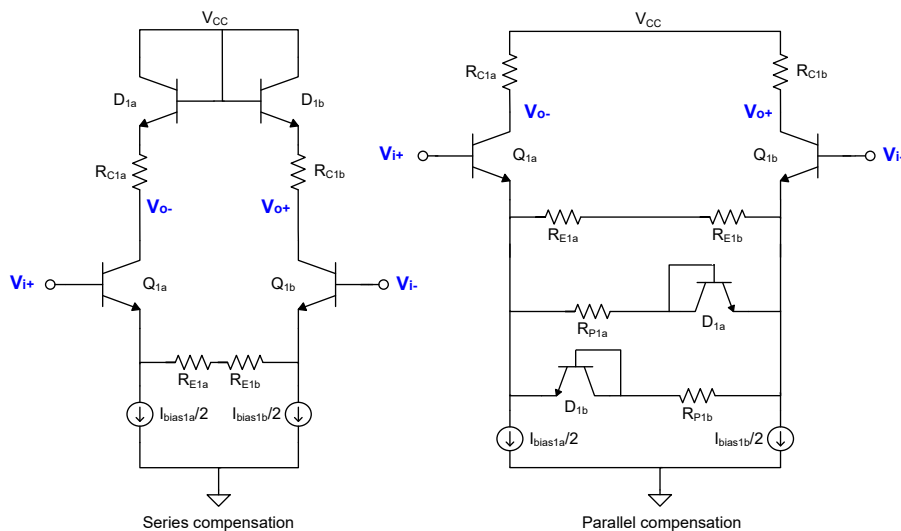
**Figure 3.** Block diagram of the L0 ASIC. All the building blocks can be disabled (en\_signals) by SPI slow control interface. The SPI interface permits also adjust the operating points of the blocks. A Power-On Reset (POR) sets known default values in the configuration registers after start-up.

**Table 1.** L0 trigger ASIC specifications.

|                                  |   |
|----------------------------------|---|
| <i>Dynamic range (input)</i>     | >20 phe per channel                           |
| <i>Bandwidth</i>                 | >500 MHz                                      |
| <i>Output noise (sum)</i>        | <2 mV RMS (with unconnected inputs)           |
| <i>Output noise (majority)</i>   | <0.2 phe (with unconnected inputs)            |
| <i>Comparator DAC resolution</i> | >8 bits                                       |
| <i>Comparator efficiency</i>     | >95%  |
| <i>Comparator purity</i>         | >99.99%                                       |
| <i>Linearity error</i>           | < $\pm 5\%$ or 0.25 phe                       |
| <i>Gain adjustment</i>           | Reduce 25% RMS amplitude dispersion to 5% RMS |
| <i>Clipping DAC resolution</i>   | >8 bits                                       |
| <i>Power consumption</i>         | <150 mW/ch                                    |

The requirements of the ASIC are summarized in table 1. The L0 trigger receives the signal from each individual PMT after signal conditioning by a preamplifier with a bandwidth larger than 350 MHz (see [11] and [12]). The L0 input signal will have an amplitude of 20 mV per phe (photoelectron) with a signal to noise ratio (S/N) larger than four. The L0 can accommodate up to 20 phe per channel. A Gaussian with 2.4 ns FWHM is a good approximation of the input signal shape.

For the majority trigger, the input signal of each pixel passes through a comparator with a programmable threshold with an 8-bit range, and is then added to the other 6 pixels that are part of the module. The comparator should be able to react fast enough to the rising edge of the input pulse that it triggers on the signal provided by one phe with an efficiency larger than 95%, while keeping



**Figure 4.** Open loop differential stage. Series (left) and parallel (right) linearity compensation.

the probability to trigger on noise below 0.01%. The output of the comparator should be a square pulse with a width equal (within  $\pm 15\%$ ) to the time the input signal was above the discriminator threshold. The linearity error of the comparator, defined as  $(\text{Mean-Fit})/\text{Fit}$ , should be at most  $\pm 5\%$  or  $\pm 0.25$  phe, whichever is larger.

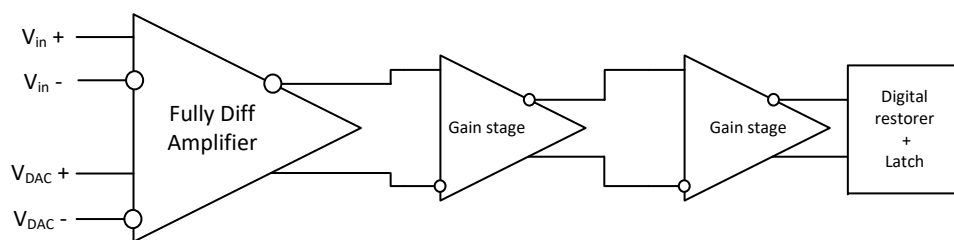
A gain adjustment is required, which does not need to be continuous. The amplitudes of the signals coming from the PMTs are expected to have an RMS deviation of around 25%. The gain adjustment should be able to reduce the amplitude spread to 5% RMS. The adjusted signal should go through a clipping block controlled by a DAC with a resolution of 8-bits or more.

Although both schemes are implemented, it is possible to power down the one that is not currently being used.

### 3.1 Basic differential stage

Several building blocks of the ASIC are based on different versions of the open loop differential stage depicted in figure 4. Those blocks comprise the input attenuators, the clipping stage, and a transconductance stage in the adders, shown in figure 3. An open loop fully differential architecture has been chosen to fulfil high-speed and low-power requirements. The main drawback of such an architecture is a moderate linearity compared with a closed loop solution. However, our linearity requirements are moderate, and closed loop (OTA/OPA based) solutions often suffer from linearity limitations due to slew rate problems.

The non-linearity of a differential pair is due to the variation of the base-emitter voltage of the two transistors. It is often corrected by the addition of one diode-connected transistor (gain of 1), as shown in figure 4 ( $D_{1a}$  and  $D_{1b}$ ), or two diode-connected transistors (gain of 2) in the collector branches to obtain the same voltage drop in the emitter and collector. However, the consequence of this “serial correction” is lower voltage headroom and that the compensation is dependent on the gain. This is problematic for low-voltage operation and for circuits with variable gain, as is the case for this ASIC. In [13], a parallel correction scheme is presented. In this parallel correction, the loss



**Figure 5.** Architecture of the discriminator.

of gain is compensated for by decreasing the emitter generation in the opposite branch, as shown in figure 4. The new linearity compensation scheme permits compensation of different gains and does not incur any penalty in voltage headroom.

### 3.2 Discriminators

The discriminator block for the majority trigger mode is based on a differential discriminator and a 10-bit digital to analogue converter (DAC) designed for the SCOTT chip ([14] and [15]). In order to maximize speed, the discriminator utilizes a multistage architecture followed by a digital restorer and a latch, as depicted in figure 5.

The DACs are differential and implement a resistor string architecture [16] to guarantee their monotonicity.

### 3.3 Adders

The fully differential adders for both the sum and majority trigger are designed as shown in figure 6. Each adder consists of seven open loop transconductance stages (one per input) and a closed loop transimpedance amplifier based on a fully differential operational amplifier. The transconductance stage is based on a degenerated differential pair with the parallel scheme for linearity compensation presented in figure 4.

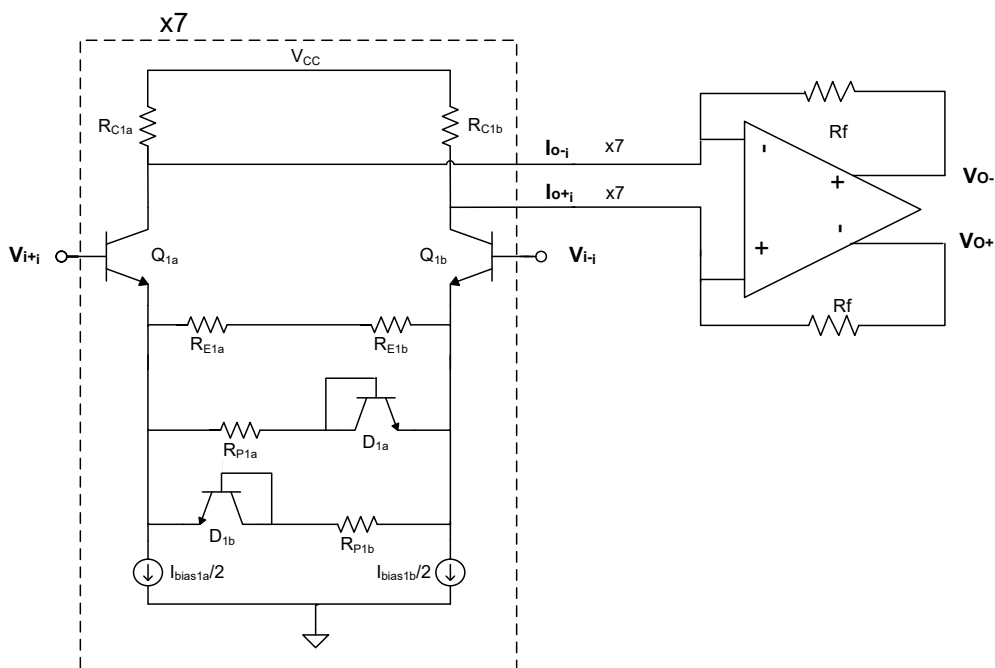
The closed loop transimpedance amplifier in figure 6 is based on a high gain-bandwidth product (GBP) operational amplifier. It is also used in other ASICs proposed for use in CTA [12]. A simplified schematic of a fully differential operational amplifier is shown in figure 7 (left). It is a folded cascode amplifier, with a second Miller stage and a class AB output stage. Miller compensation is used with a nulling resistor. The input pair is degenerated to improve slew rate. Fast and accurate common-mode feedback is continuously provided by an error amplifier.

The class AB output stage is shown in figure 7 (right). The push-pull operation is based on a fast local feedback loop, where the GBP exceeds 2 GHz with a phase margin (PM) exceeding 60 deg. This stage can provide more than 20 mA peak current, with a quiescent current of 5 mA. This allows driving low load impedances with AC coupling, i.e., the cable or transmission line impedance connecting the L0 ASIC to the trigger backplane, as shown in figure 1.

### 3.4 A 7-channel ASIC

The ASIC is implemented in a 0.35  $\mu\text{m}$  BiCMOS technology with SiGe NPN HBTs. The use of heterojunction bipolar transistors (HBTs) is required for several reasons:





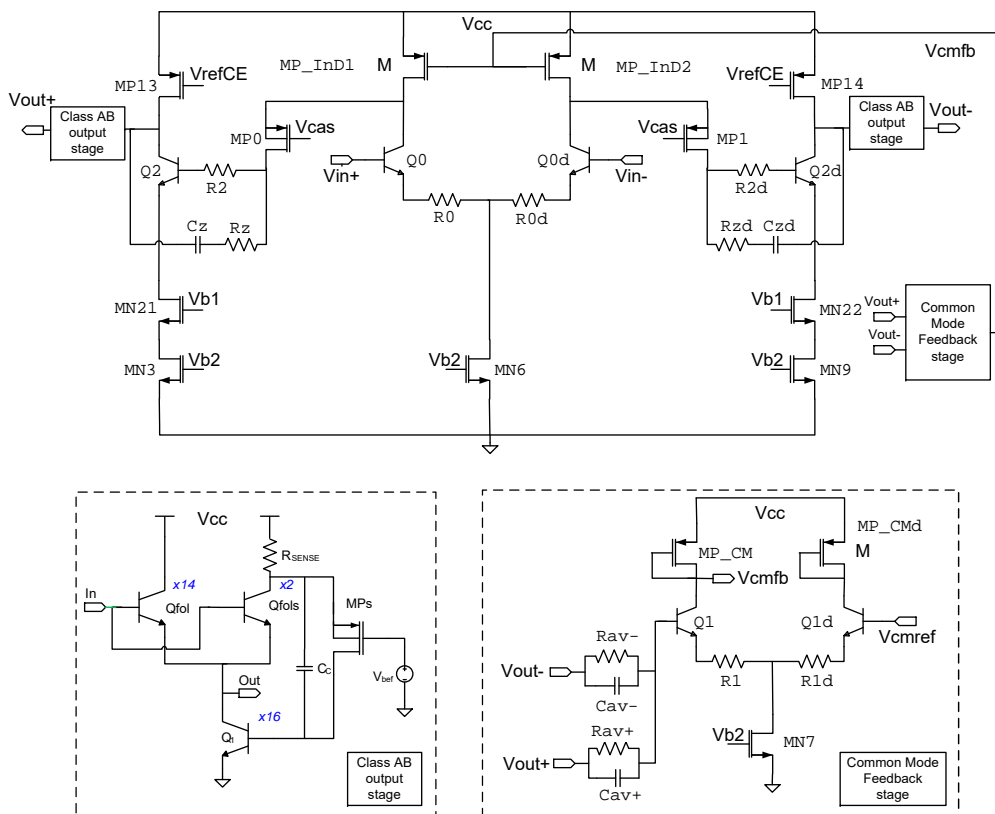
**Figure 6.** Schematic of the adder block. Dashed box corresponds to the degenerated differential pair with the parallel scheme for linearity compensation presented in figure 4. Closed loop transimpedance amplifier in the right.

- The bandwidth (BW) of the signal processing in the ASIC must be higher than 500 MHz. This means that the bandwidth of each stage should be significantly higher, 700 MHz or more. Therefore, the use of active devices with high unity-gain frequency  $f_t$  is crucial.
- The differential pair stages depicted in figure 4 and figure 6 rely on emitter degeneration to achieve the required linearity. Bipolar devices provide a very good transconductance over bias current ratio.

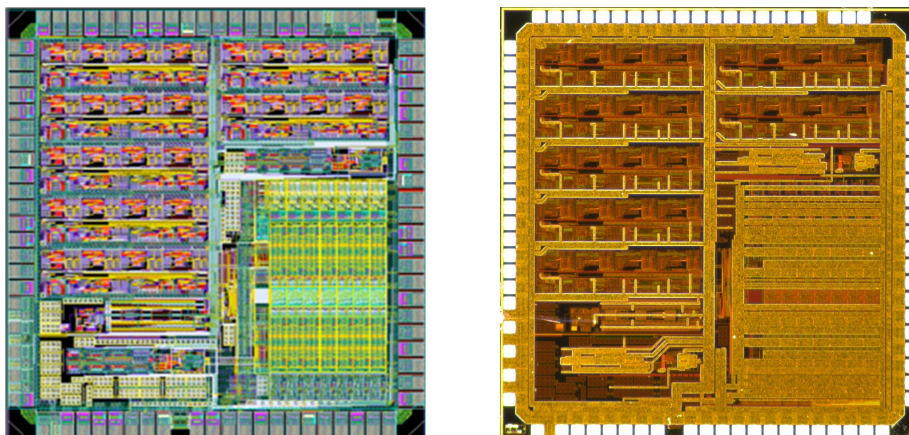
The layout and microphotograph of the ASIC are shown in figure 8. The area is about  $12 \text{ mm}^2$  and it is packaged in a QFN 56 package. Three different simultaneous operation modes are possible: sum trigger, majority trigger, and a digital trigger with the seven discriminated LVDS outputs. The subsystem corresponding to each mode can be set in “power down” mode independently for each individual channel. The chip can be configured and the operating parameters (thresholds, attenuation factors, bias currents, etc.) set by means of a Serial Peripheral Interface (SPI) bus. The power consumption depends on the ASIC configuration, but consumption for either sum or majority trigger operation is typically about 90 mW per channel.

## 4 Results

The L0 ASIC has been integrated in the NECTAr and DRAGON front end (FE) boards [17]. A typical L0 ASIC sum trigger output for a 2 phe signal using the DRAGON FE board is shown in figure 9.

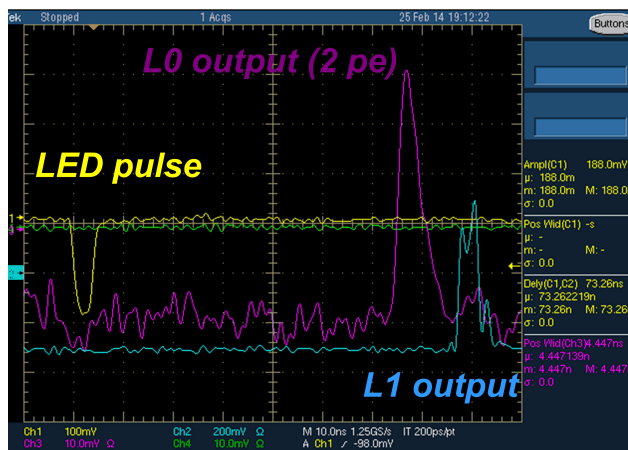


**Figure 7.** Simplified schematic of the fully differential operational amplifier (top). At the bottom: the class AB output stage (bottom-left) and common mode feedback stage (bottom-right). The substrate of all N-MOS transistors is tied to ground. The substrate of all P-MOS transistors is tied to VDD unless explicitly indicated.

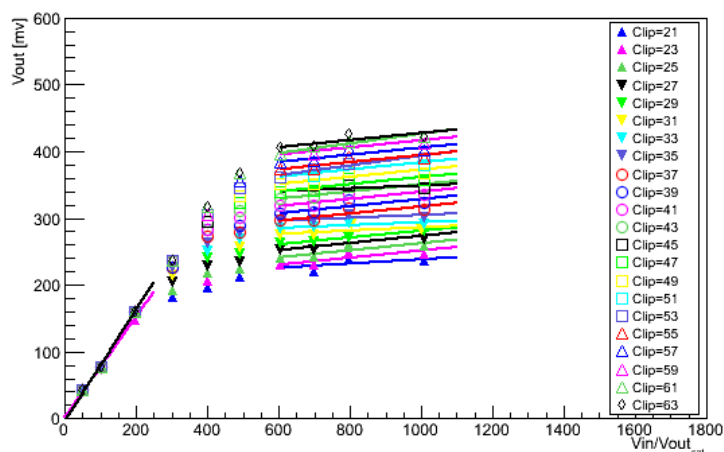


**Figure 8.** Layout (left) and microphotograph (right) of the ASIC.

The response of the sum trigger system for different clipping levels is depicted in figure 10. The system is linear until a saturation or clipping level is reached. The clipping level is a configurable parameter.



**Figure 9.** Typical L0 ASIC sum trigger output for a 2 phe signal using DRAGON FE.

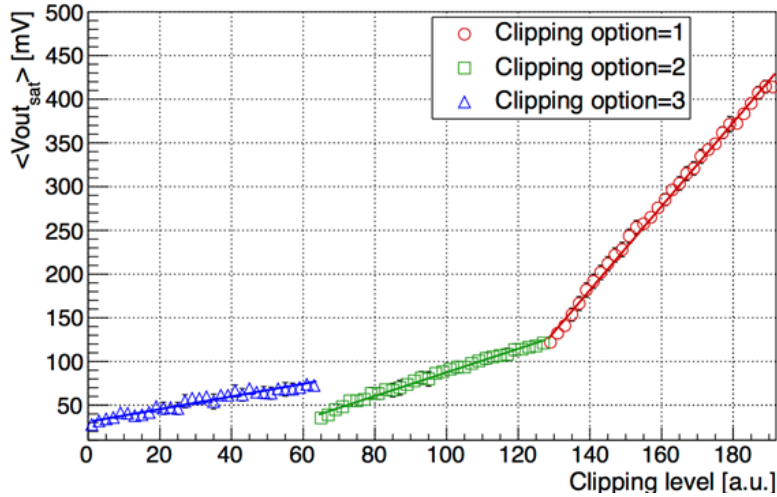


**Figure 10.** Sum trigger transfer function for different fine clipping levels. Fine clipping is encoded in a 6-bit word, so the fine clipping range is between 0 and 63.

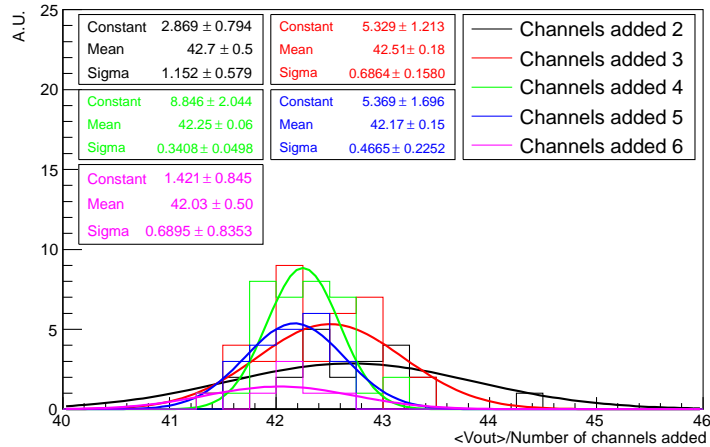
The clipping level can be adjusted from 30 to 450 mV, as shown in figure 11. Three different ranges can be selected by a coarse control (2 bits). A fine control (6 bits) sets the precise level of clipping for each channel.

The performance of the sum trigger adder is illustrated in figure 12. For a given attenuation and clipping, we measured the output of the adder. We used an input signal of 50 mV and a high clipping value in order to not clip the signals at the output. We measured the output of the adder for all the possible combinations of channels added. We histogrammed the measured outputs of the adder (divided by the number of channels added) for each number of channels added. Since the inputs for each channel are identical, the ratio of the adder's output voltage to the number of channels added should be the same in all cases. The histograms are fit with Gaussian functions whose standard deviations are at the level of 1–2% of the mean.

The linearity of the majority trigger discriminator will partially determine how accurately a telescope's energy threshold (an important quantity) can be measured. Discriminator linearity was



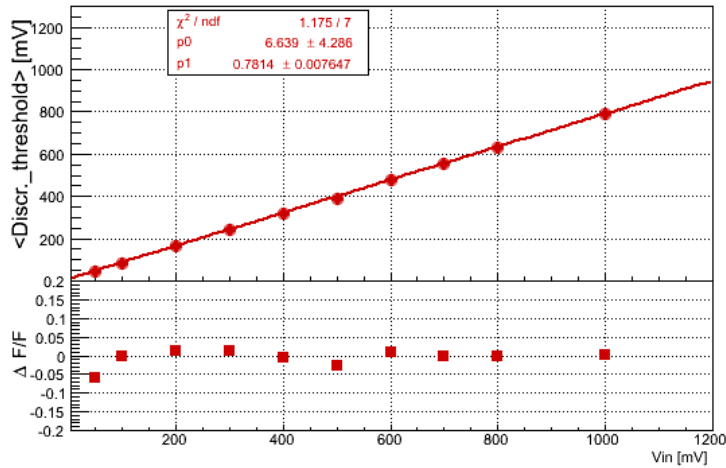
**Figure 11.** Output voltage saturation level plotted as a function of clipping level (coarse and fine). Coarse control allows setting 3 different clipping regions (labelled clipping options in the plot).



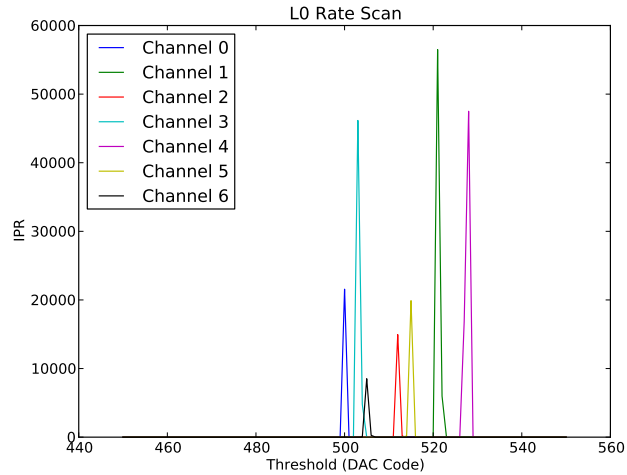
**Figure 12.** Output of the sum adder divided by the number of channels added for an input signal of 50 mV. Histograms for the different number of channels added are shown in different colors (2 channels in black; 3 channels in red; 4 channels in green; 5 channels in blue; 6 channels in magenta) and fit with a Gaussian, represented by a line of the same color as the histogram. The results of the fit are shown in the plot with the same color as the fit.

measured by determining the mean discriminator threshold (DT) of all the channels for a given input amplitude and attenuation. We define the DT for each channel as the discriminator voltage for which the output signal goes to zero. The DTs should increase linearly with the input voltage. A linear fit of the mean DT as a function of the input, as well as the residuals, is shown in figure 13. The residuals indicate that the majority trigger discriminator is linear within  $\sim 5\%$  over the entire dynamic range.

The noise of the majority chain can be inferred from the curves resulting from the threshold scans. The trigger rate as function of the threshold value for the seven channels of an ASIC is depicted in figure 14.



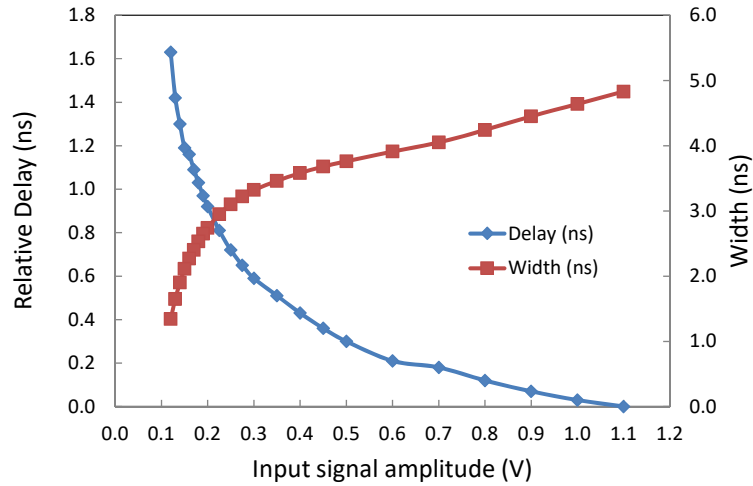
**Figure 13.** Discriminator transition for different input signal amplitudes. Linear fit (top) and residuals (bottom) are shown.



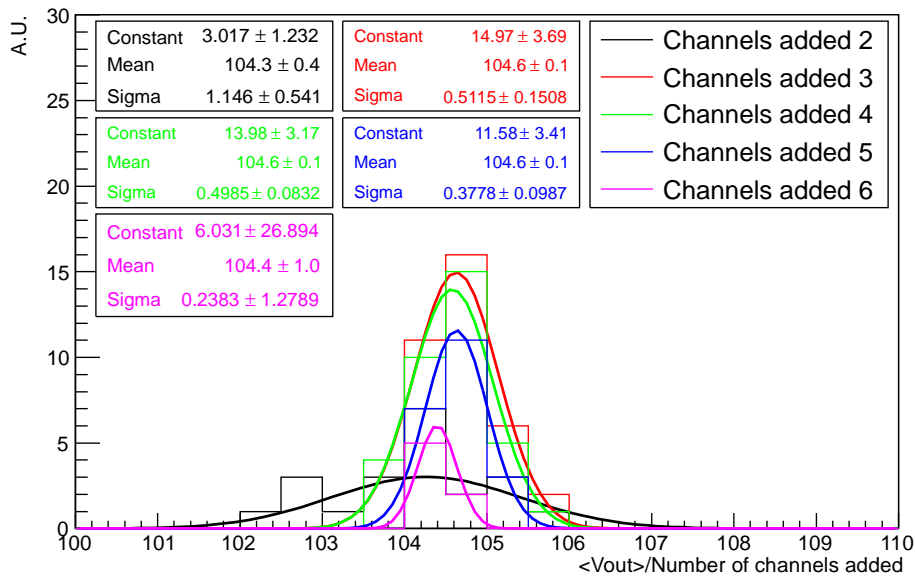
**Figure 14.** Trigger individual pixel rate (IPR) as function of discriminator threshold for the 7 channels of an L0 ASIC. The noise is about 1 mV RMS, well below the 0.2 phe requirement.

The majority trigger timing characteristics are shown in figure 15. Relative delay (from input to output) variation and output pulse width are measured as a function of input signal amplitude. The input pulse FWHM is about 3 ns. The threshold is set to about 6 phe, and the approximate calibration is 20 mV/phe at the input of the L0 ASIC. The discriminator propagation delay and time walk are well below 2 ns.

The performance of the majority adder is illustrated in figure 16. In this case, the discriminator outputs are added. For a given attenuation, we measured the addition of all the possible combinations of channels. The final output was divided by the number of channels added to fill different histograms, depending on the number of channels added. The histograms were fitted with Gaussian functions with standard deviations of  $< 1\%$  of the mean normalized output voltage.



**Figure 15.** Majority trigger timing characteristics. Relative delay variation (blue) and output pulse width (red) are plotted as a function of input signal amplitude (input FWHM is about 3 ns). The threshold is set to about 6 phe, with 20 mV/phe at the input of the L0 ASIC.



**Figure 16.** Output of the majority adder divided by the number of channels added. Histograms for the different number of channels added are shown in different colors (2 channels in black; 3 channels in red; 4 channels in green; 5 channels in blue; 6 channels in magenta) and fit with a Gaussian, represented by a line of the same color as the histogram. The results of the fit are shown in the plot with the same color as the fit.

## 5 Conclusions

We have presented a versatile and reconfigurable ASIC for triggering Cherenkov telescope cameras. The ASIC implements two different analogue trigger schemes: the sum trigger and the majority trigger. Furthermore, the discriminator outputs are available as independent LVDS signals, allowing

for the implementation of complementary digital trigger schemes, such as the FPGA-based digital trigger presented in [17].

Unused blocks in a given operation mode can be individually set in standby mode, thus optimizing the power consumption, which is a factor of five smaller than equivalent solutions implemented with commercial off-the-shelf components [6].

A combination of open and closed loop design techniques is used to achieve high speed and minimize power consumption, while fulfilling linearity and noise requirements. Fully differential design is used to increase power supply noise rejection and to increase dynamic range.

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