Efficiency and reliability enhancement of silicon nanocrystal field-effect luminescence from nitride-oxide gate stacks

M. Perálvarez,[1,a)] Josep Carreras,[1] J. Barreto,[2] A. Morales,[2] C. Domínguez,[2] and B. Garrido[1]
[1]*EME/IN²UB, Departament d'Electrónica, Universitat de Barcelona, Martí i Franquès 1, 08028 Barcelona, Spain*
[2]*Instituto de Microelectrónica de Barcelona (IMB-CNM, CSIC), Bellaterra 08193, Barcelona, Spain*

(Received 31 March 2008; accepted 16 May 2008; published online 17 June 2008)

We report on a field-effect light emitting device based on silicon nanocrystals in silicon oxide deposited by plasma-enhanced chemical vapor deposition. The device shows high power efficiency and long lifetime. The power efficiency is enhanced up to ~0.1% by the presence of a silicon nitride control layer. The leakage current reduction induced by this nitride buffer effectively increases the power efficiency two orders of magnitude with regard to similarly processed devices with solely oxide. In addition, the nitride cools down the electrons that reach the polycrystalline silicon gate lowering the formation of defects, which significantly reduces the device degradation. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2939562]

The materials based on silicon nanocrystals (Si-ncs) are attractive for a wide variety of electronic and optoelectronic applications thanks to their tunable emission in the visible range and their compatibility with mainstream complementary metal oxide semiconductor (MOS) technology.[1–6] In the last years, an increasing number of articles dealing with electroluminescence (EL) from Si-nc embedded in silicon oxide (Si-nc/SiO_2) devices has been published. Many of them report emission under direct current (dc) polarization,[7–9] which usually leads to low emission efficiency and fast degradation. Other authors report emission under alternate current (ac) polarization,[3,10,11] applying the concept of field-effect luminescence, where the recombination takes place after the sequential injection from the substrate of electrons and holes. The alternate injection can be adjusted to a suitable duty cycle which optimizes not only the current flow but also the polarization stress and the device lifetime. In spite of this, the leakage current is still very high and, also in this case, leads to low power efficiencies.[10] Therefore, the reduction of the leakage current appears to be a key issue for the achievement of an efficient device. In this challenge, the addition of a thin silicon nitride (Si_3N_4) layer in a typical metal nitride-oxide semiconductor (MNOS) configuration is presented as a promising solution.[12–14] The MNOS stack reduces the effective field in the oxide layer, lowering the current flow that, in MOS configurations, is strongly field dependent [Fowler–Nordheim (FN)].[15] The additional nitride barrier hinders the gate injection without significantly affecting the injection from the substrate, thus enhancing the power efficiency, as will be demonstrated later on. Thanks to the thinness of the Si_3N_4 buffer and to its relatively high dielectric constant, the overall thickness increase does not have a remarkable impact on the gate voltage. The device lifetime improves as the nitride matrix cools down the carriers from the oxide, reducing the damage generated at the polycrystalline silicon (top contact) interface.

In the present work, we demonstrate a twofold improvement through the addition of a thin Si_3N_4 control layer within the MOS stack. First, we show that the power efficiency is increased up to ~0.1% (two orders of magnitude larger than the one obtained in identically processed MOS structures) as a direct consequence of the leakage current reduction that takes place for comparable voltages and output emitting powers. Second, measurable reduction of the device degradation is also demonstrated.

Two different types of metal-insulator-semiconductor structures have been fabricated. The first one is a MNOS structure with a pure nitride ~15-nm-thick control layer deposited onto an ~55 nm Si-nc/SiO_2 layer with roughly ~20% of Si excess, which plays the role of active layer. The second set of devices presents a typical MOS configuration with the same oxide thickness (~55 nm) and similar Si excess. The silicon-rich silicon oxide layers were deposited on a *p*-type Si substrate (0.1–1.4 Ω cm) by plasma-enhanced chemical vapor deposition (CVD) and submitted to high temperature annealing. More experimental details are given elsewhere.[10] The addition of the nitride layer was performed by low-pressure CVD at 800 °C and 26.66 Pa with a NH_3 (ammonia) and SiH_2Cl_2 (dichlorosilane) mixture. N-doped semitransparent polycrystalline silicon (poly-Si) 250 nm thick was deposited as a contact layer on both samples. Transmittance spectroscopy of poly-Si layers deposited onto fused silica wafers was performed in order to check its transparency. Finally, aluminum pads were deposited for an easier probe connection. The devices were biased by bipolar square waves from an Agilent 8114A Pulse Generator. Time-resolved EL was detected by a photon-counting setup basically composed of a Hamamatsu H7422-50 photomultiplier. The EL spectra were measured by a Princeton Instruments 100B-LN charge coupled device camera and an Oriel MS257 1/4 m Monochromator. Quasistatic *I-V* (current-voltage) characteristics were measured by an Agilent B1500 semiconductor device analyzer.

The schematics of Fig. 1(a) show some basic principles of MNOS structures. The nitride buffer reduces the applied field in the oxide (barrier height increase), leading to a decrease in the current density (i). Diagrams (ii) and (iii) represent the probabilities of electron injection from the gate

a)Electronic mail: mperalvarez@el.ub.es.

 © 2008 American Institute of Physics
Downloaded 24 Mar 2010 to 161.116.95.217. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

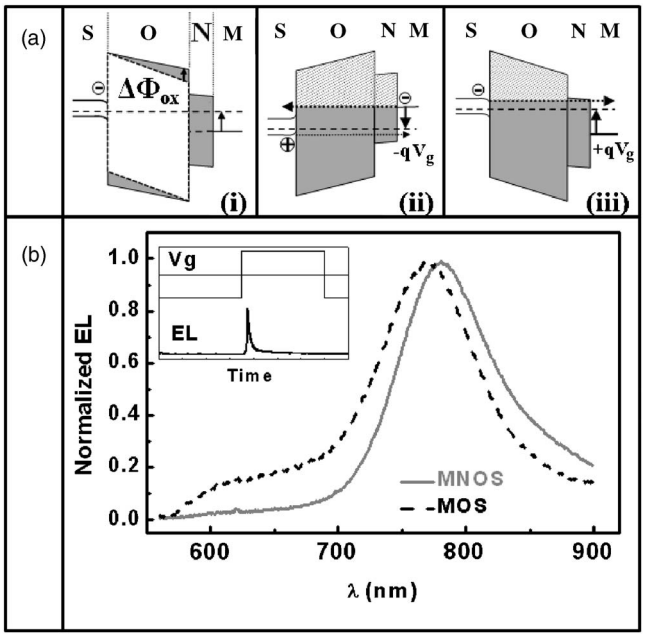

FIG. 1. (a) Band structure of MNOS devices. (i) The oxide barrier increases due to the control layer addition. [(ii) and (iii)] The probability of carrier injection from the substrate is higher than that for gate injection as revealed by the different lighted areas which are related to the inverse of the injection probability. (b) Comparison of EL spectra from MOS and MNOS structures. In the inset, a typical time-resolved scheme of the field-effect emission is represented.

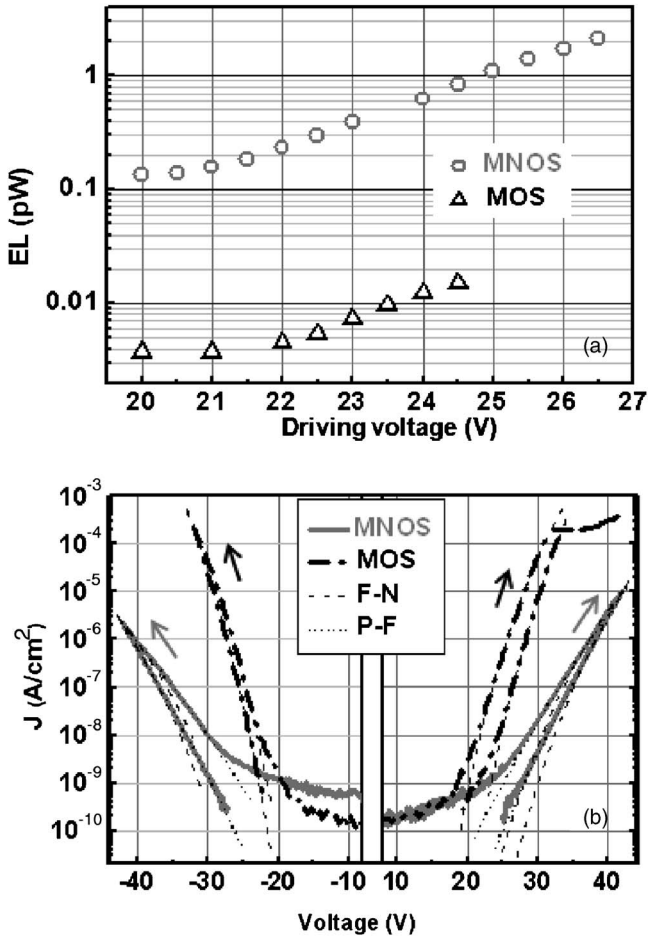

FIG. 2. (a) Integrated field-effect luminescence as a function of the driving voltage. (b) Current-voltage characteristics of MNOS and MOS devices, together with the corresponding injection models (fittings). The arrows indicate the forward sweep direction.

and the substrate, respectively, which are related to the inverse of the lighted areas. Whereas the nitride barrier strongly hinders the carrier injection from the gate, (ii), its influence on the substrate injection, responsible of the field-effect luminescence, is negligible (iii). Figure 1(b) represents the field-effect luminescence spectra of MNOS and MOS devices under application of 26 V square wave voltages. As represented in the inset, most of the emission is triggered by the rise edge of the applied voltage, when the electrons are injected into positively charged Si-nc. The contribution of the fall-edge transient is very small, mainly due to the shorter retention times of the previously stored electrons.[11] In both cases, the rise time of the emission is around 0.2 μs, whereas the decay time is close to 10 μs. The spectra have been normalized to their own maxima in order to make easier the comparison of their spectral features. The emission range matches the typical Si-nc/SiO_2 emission.[2,3] The spectral shapes are very similar, even though their full width at half maximum is narrower (close to ~90 nm, i.e., ~0.190 eV) than the one obtained in similar samples under optical pumping.[16] This can be attributed to interference effects caused by multiple reflections in the poly-Si layer, as revealed by transmittance measurements (figure not shown). The small peak shift is attributed to the different refractive index contrast at the poly-Si/insulator interface that modifies the interference pattern of the stack. Figure 2(a) shows the integrated EL for both devices as a function of the driving voltage. It is worth noting that, in both cases, the onset of the emission is placed at about ~20 V, indicating that the nitride layer does not have a sizable impact on the operation voltage. This agrees with the relatively small estimated voltage drop in the nitride layer (~14% of the gate voltage) and the similarity in the current values measured at the onset of the emission [see Fig. 2(b)]. The quasistatic current-voltage measurements show a strong reduction of the current in MNOS structures compared to MOS devices. This reduction represents the base of the power efficiency improvement, as we demonstrate hereafter. In conventional MNOS structures (without Si-nc), the overall current is the result of the balance between two different injection mechanisms that take place in the SiO_2 and the Si_3N_4. The measured gate current is ruled by the less conductive layer, role defined by the device characteristics. This current consists of carriers tunneling from the substrate to the oxide conduction band by FN mechanism and being trapped at the oxide-nitride interface where the carriers are promoted to the poly-Si contact by Poole–Frenkel (PF) mechanism.[12,13,17] In our devices, the current can be interpreted in a similar way, even though the FN tunneling is now assisted by the Si-nc. Figure 2(b) reveals that above ~20 V (emission range), the current in MNOS devices can be separated in two different regimes. Close to the threshold voltage, the current is well fitted by PF injection, implying that in this *I-V* region, the nitride layer plays the role of limiting layer. As the voltage is further increased, the Fermi level of the Si substrate raises, overcoming the nitride conduction band and promoting the carriers to the gate without "seeing" the nitride layer. As extracted from Fig. 2(b), the overall current in this range follows a FN law with typical barrier heights of 1.6–1.9 eV, in good agreement with values obtained from FN fittings in MOS structures with Si-nc (from 1.8 to 2.2 eV). If one assumes

Downloaded 24 Mar 2010 to 161.116.95.217. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

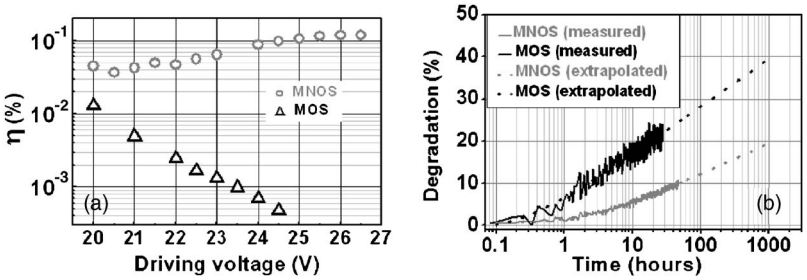

FIG. 3. (a) Power efficiency as a function of the applied voltage for MNOS and MOS devices. (b) Fraction of light intensity decrease (degradation) as a function of the operation time, as measured and as extrapolated.

that the FN current through the oxide in the MNOS structure is approximately the same than that measured for the MOS structure, then Fig. 2(b) demonstrates the current reduction induced by the nitride layer. This assumption is justified by the small estimated voltage drop in the silicon nitride (~14%) and the small variation of the effective barrier height, calculated from the *I-V* hysteresis, which is about 10% of the calculated height. The low current level involved results into high power efficiencies, as represented in Fig. 3(a). The MNOS structure exhibits a mean power efficiency of about ~0.1% that slightly varies in a broad range of voltages. This behavior differs from the one observed in MOS structures, where the benefit in the output optical power by increasing the gate voltage does not compensate the electrical power dissipation, due to the high leakage current flowing through the stack. Taking also into account the different emission intensities observed in Fig. 2(a), it becomes clear that the benefit of the nitride layer is twofold, as not only it reduces the device current flow but also improves the luminescence intensity. This implies a better profit of the injected charge, which is the basis of the efficiency enhancement.

The structures were submitted to accelerating aging for more than 24 h of continuous operation under application of 30 V bipolar square waves at 1 kHz. The emission intensity from MNOS structures slowly decreased, attaining a relatively high emission level, ~91%. In contrast, the emission from MOS devices dropped to ~79% of its original value. This demonstrates a general improvement of the device endurance under alternate biasing, underlining the superior reliability of MNOS structures, compared to MOS. This improvement is clearly shown in Fig. 3(b), where the degradation is represented as function of the operation time. The degradation rate in MNOS is about ~50% slower than that observed in MOS devices, so that the resulting lifetime is considerably longer. This trend is well fitted by a logarithmic function of time within the experimental timescale,[18] and results in extrapolated device lifetimes of few months.

In conclusion, the fabrication of Si-nc based devices with a thin silicon nitride layer enhances the power efficiency up to 0.1%. This increase is mainly due to the reduction in the leakage current that not only favors a decrease in the power consumption but also enhances the injection to the Si-nc. The control layer has no noticeable effect on the threshold voltage, due to the high dielectric constant and the thinness of the added layer. MNOS LEDs show a significant increase of the endurance, reducing the degradation rate down to 50%.

This work was partially supported by the project MILES-SILUZ: TEC2006-13907/MIC, financed by the Spanish Ministry of Education and Science. A. Morales and J. Barreto acknowledge the grants received from CONACyT-FC and CSIC (I3P), respectively. M. Perálvarez acknowledges Dr. Paolo Pellegrino.

[1] L. Pavesi and D. J. Lockwood, *Silicon Photonics, Topics in Applied Physics* (Springer, Berlin, Germany, 2004), Vol. 94, pp. 1–52.
[2] J. Carreras, J. Arbiol, B. Garrido, C. Bonafos, and J. Monserrat, Appl. Phys. Lett. **92**, 091103 (2008).
[3] R. J. Walters, H. Atwater, and G. Bourianoff, Nat. Mater. **4**, 143 (2005).
[4] M. Porti, M. Avidano, M. Nafría, X. Aymerich, J. Carreras, O. Jambois, and B. Garrido, J. Appl. Phys. **101**, 064509 (2007).
[5] G. Vijaya Prakash, M. Cazzanelli, Z. Gaburro, L. Pavesi, F. Iacona, G. Franzó, and F. Priolo, J. Appl. Phys. **91**, 4607 (2002).
[6] R. J. Walters, P. G. Kik, J. D. Casperson, H. A. Atwater, R. Linsdtedt, M. Giorgi, and G. Bourianoff, Appl. Phys. Lett. **85**, 2622 (2004).
[7] L. Rebohle, J. von Borany, R. Grötzschel, A. Markwitz, B. Schmidt, I. E. Tyschenko, W. Skorupa, H. Fröb, and K. Leo, Phys. Status Solidi A **165**, 31 (1998).
[8] A. Irrera, F. Iacona, G. Franzo, S. Boninelli, D. Pacifici, M. Miritello, C. Spinella, D. Sanfilippo, G. Di Stefano, P. G. Fallica, and F. Priolo, Opt. Mater. (Amsterdam, Neth.) **27**, 1031 (2005).
[9] J. De La Torre, A. Souifi, A. Poncet, C. Busseret, M. Lemiti, G. Bremond, G. Guillot, O. González, B. Garrido, J. R. Morante, and C. Bonazos, Physica E (Amsterdam) **16**, 326 (2003).
[10] M. Perálvarez, C. García, M. López, B. Garrido, J. Barreto, C. Domínguez, and J. A. Rodríguez, Appl. Phys. Lett. **89**, 051112 (2006).
[11] R. J. Walters, J. Carreras, T. Feng, L. D. Bell, and H. A. Atwater, IEEE J. Sel. Top. Quantum Electron. **12**, 1647 (2006).
[12] P. Gentil, *Silicon Passivation and Related Instabilities*, edited by G. Barbouttin and A. Vapaille (Elsevier Science, Amsterdam, 1986), Vol. 2, p. 659.
[13] C. G. Parker, G. Lucovsky, and J. R. Hauser, IEEE Electron Device Lett. **19**, 106 (1998).
[14] A. Sudhakar Reddy, P. R. S. Rao, K. N. Bhat, and N. D. Gupta, Proc. SPIE **3975**, 357 (2000).
[15] E. Kameda, T. Matsuda, Y. Emura, and T. Ohzone, Solid-State Electron. **42**, 2105 (1998).
[16] F. Iacona, G. Franzó, and C. Spinella, J. Appl. Phys. **87**, 1295 (2000).
[17] H. Tanaka, Appl. Surf. Sci. **147**, 222 (1999).
[18] Z. Cui, J. J. Liou, and Y. Yue, IEEE Trans. Electron Devices **50**, 1398 (2003).

Downloaded 24 Mar 2010 to 161.116.95.217. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp