Auger quenching-based modulation of electroluminescence from ion-implanted silicon nanocrystals

Josep Carreras[1], C Bonafos[2], J Montserrat[3], C Domínguez[3],J Arbiol[1], and B Garrido[1]

[1] IN^{2}UB-EME, University of Barcelona. C/Marti i Franques 1, PL2, 08028 Barcelona, Spain

[2] CEMES-CNRS, nMat Group, 29 rue J. Marvig, 31055 Toulouse, France

[3] IMB-CNM, CSIC, Bellaterra 08193, Barcelona, Spain

E-mail: carreras@el.ub.es

Abstract. We describe high-speed control of light from silicon nanocrystals under electrical excitation. The nanocrystals are fabricated by ion implantation of Si^+ in the 15-nm-thick gate oxide of a field effect transistor at 6.5 keV. A characteristic read-peaked electroluminescence is obtained either by DC or AC gate excitation. However, AC gate excitation it is found to have a frequency response that is limited by the radiative lifetimes of silicon nanocrystals, which make impossible the direct modulation of light beyond 100 Kb/s rates. As a solution, we demonstrate that combined DC gate excitation along with an AC channel hot electron injection of electrons into the nanocrystals may be used to obtain a 100%-deep modulation at rates of 200 Mb/s and low modulating voltages. This approach, may find applications in biological sensing integrated into CMOS, single-photon emitters, or direct encoding of information into light from Si-nc doped with Erbium systems, which exhibit net optical gain. In this respect, the main advantage compared to conventional electro-optical modulators based on plasma dispersion effects is the low power consumption (10^5 times smaller) and thus the inherent large scale of integration. A detailed electrical characterization is also given. A Si/SiO_2 barrier change from Φ_b=3.2 eV to 4.2 eV is found while the injection mechanism is changed from Fowler-Nordheim to Channel Hot Electron, which is a clear signature of nanocrystal charging and subsequent electroluminescence quenching.

PACS numbers: 73.63.Bd, 78.67.Bf, 85.60.Jb

Submitted to: *Nanotechnology*

1. Introduction

Silicon nanocrystal (Si-nc) based devices have recently attracted much attention for a wide range of applications, including non-volatile memories[1], light emitting devices[2, 3, 4, 5, 6, 7] and luminescence sensitizers of dopants such as Erbium[8]. A success in obtaining Erbium population inversion and net signal gain in the latter application would allow the realization of an all-silicon laser (either with optical or electrical pump), which is highly desirable for silicon photonics. However, Si-nc have not been considered as good candidates for high-speed applications[4] due to the limitation imposed by their characteristic radiative lifetimes, which make them transparent for excitation frequencies higher than a few kilohertz. This fact forces light modulators for silicon photonics being designed as independent elements that receive light from a constant external source to output a pulsed beam according to a pattern of information to be transmitted[9, 10, 11, 12]. The majority of nowadays state-of-the-art silicon electro-optical modulators are based on plasma dispersion effects[12]. Unfortunately, they suffer from high power consumption (theoretical lower limit of current density 10^4 A/cm^2)[11] and poor scalability. In regard to light emitting sources, Si-nc are still promising and recent developments have demonstrated tuneable emission after doping with carbon[3, 13] and efficient emission under single-electrode sequential excitation[14].

In this paper, we describe in detail the principles of operation of a solution that provides Si-nc emission along with high modulation rates. This implies that efficient emission from Si-nc is generated and modulated within the same device, which will be termed throughout this paper as direct modulation[15], in contrast to electro-optical modulation[9, 10, 11, 12], through which information is encoded into light from an external source. Potentially, the applications that such a solution may offer are two-fold. On one hand, modulation of the broad emission of Si-nc is fully integrated in a MOSFET, which enables the possibility to enlighten silicon chips in emerging niche applications, were laser-based communications is not yet required (i.e. on-chip detection or sensing but not LAN), bringing forth new geometries and designs. Compared to stand-alone electro-optical modulators, the small voltages and low power consumption required for a high-depth modulation make this approach further attractive. On the other hand, having a good control of the recombination mechanisms that are available on a Si-nc during electrical excitation, opens the possibility to foresee Si-nc as engineered sensitizers, in which the availability of the excitonic energy can be obtained on-demand, fully controlling and optimizing the energy transfer process, which is an unsolved necessary condition for population inversion and consequently for silicon-compatible lasing.

The emission of nanocrystals in our device is generated by field effect excitation through a gate direct current (DC). We study the two methods that our device offers to electrically modulate the luminescence; i) modulation by suppression of the Fowler-Nordheim (FN) gate excitation and ii) modulation by Channel Hot Electron (CHE) injection of the continuous FN gate emission. In agreement with frequency responses

from the literature[14], the first method it is shown to be too slow to have an impact in communications because it is ultimately limited by radiative rates of nanocrystals. The second option makes use of the full potential of the MOSFET structure, utilizing CHE injection, an efficient charge injection mechanism used to program flash memories, to suppress the luminescence by enabling alternative non-radiative paths in the decay process, without removing the gate excitation. This new second option it is shown to be very promising for high-speed transfers, as increases the modulation speed at least three orders of magnitude compared to gate modulation. The electrical properties will be discussed in a final section in this paper, providing supporting data to the optical results.

2. Experimental

The device structure resembles that of a Si-nc memory[1], a MOSFET with a floating gate embedded into the gate oxide made up of Si-nc (figure 1a). There are two fundamental differences, though. First, provided that impact excitation occurs, there is no need for a minimum tunnel oxide thickness, as charge retention is not pursued in the present device. This implies that the distribution of Si-nc along the oxide is targeted close to the substrate/SiO_2 interface. Since tunnelling rates strongly depend on dielectric thicknesses, a fast carrier injection may be expected. Secondly, the thickness of the polycrystalline silicon layer used for the gate contact has been reduced to allow optical transparency in the spectral range of interest.

MOSFET transistors with 100 nm-thick optically transparent and polycrystalline silicon gate electrodes with embedded Si-nc in the gate oxide were fabricated. The nanocrystals were obtained after 6.5 keV Si^+ ion implantation into thermally grown SiO_2 15-nm-thick layers and resulted in atomic Si peak excess of 20% at a projected range of ∼12 nm, as simulated by SRIM[16] code. The samples subsequently underwent an annealing in N_2 at 1100 °C. The thermal budget used ensured the precipitation of all the implanted Si and a complete phase separation. A phosphorus implantation was used to define source and drain zones. A polycrystalline silicon layer was deposited by Low-Pressure Chemical Vapour Deposition (LPCVD) and degenerately doped with $POCl_3$ to form a semitransparent gate electrode. Standard microelectronic processes of photolithography and etching were used to form the transistor structure.

The atomic Si peak excess of silicon inside the matrix was confirmed to be 20% by X-ray Photoelectron Spectroscopy (XPS). Energy Filtered Transmission Electron Microscopy (EFTEM) technique was used to confirm the dimensions of the structure as shown in figure 1b. The presence of Si-nc in the oxide was further verified by EFTEM at a Si plasmon energy of ∼17 eV. Silicon nanocrystals were imaged at an average distance of 10.5 nm (distance from gate to centre of nanocrystal layer). The diameter of the observed nanocrystals was 4-5 nm, but a reliable size distribution could not be extracted due to a limited statistics.

Time-resolved EL traces were obtained with a thermo-electrically cooled

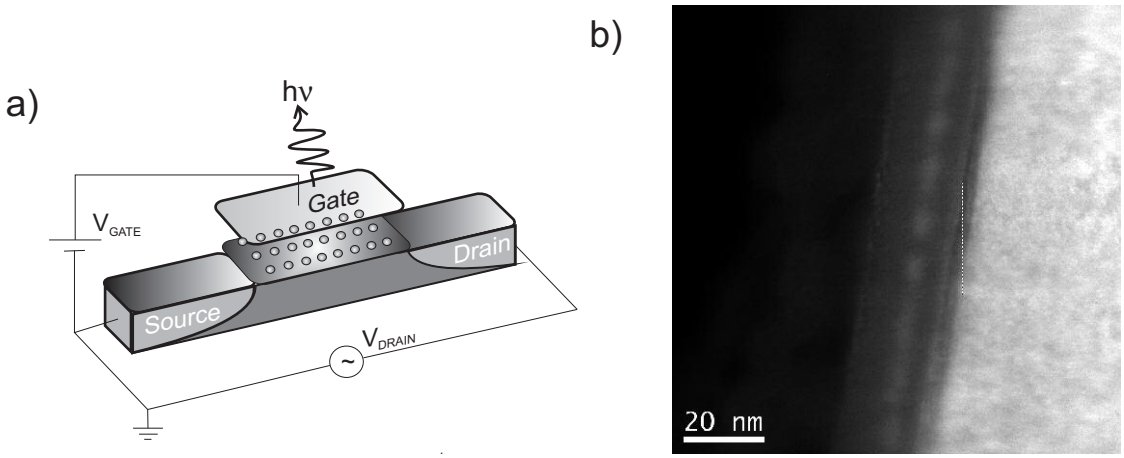

Figure 1. (a) Device schematics. (b) Energy Filtered Transmission Electron Microscopy of the structure showing a single-layer of silicon nanocrystals embedded in the gate oxide close to the substrate.

Hamamatsu H7422P detector (spectral response from 380 to 890 nm), a Stanford Research SR445A 350 MHz preamplifier and a SR430 Multichannel Scaler-Averager. The overall experiment was driven by MATLAB and synchronously triggered by an Agilent 8114A pulse generator. Electrical excitation was carried out through an Agilent 33220A (20 MHz) function generator for the gate and an Agilent 8112A (50 MHz) for the drain contacts. Light emerging from the gate region was collected with a Seiwa 888L microscope embedded in the probe station and directed through internal lens to the detector active area. Electroluminescence spectra were obtained with a cryogenically cooled Princeton Instruments Spec-10-100B/LN charge-coupled device and an Acton 2300i grating spectrometer. Data were corrected with the overall optical transfer function. Electrical characterization of the transistors was performed with a semiconductor device analyzer (Agilent B1500) and a probe station (Cascade Microtech Summit 11000).

3. Electroluminescence modulation

3.1. Constant Fowler-Nordheim gate excitation

Figure 2 shows the EL spectrum obtained by a constant field effect excitation. From the position and shape of the emission distribution and typical lifetimes analyzed later on, the emission is attributed to Si-nc. Identical control samples without embedded Si-nc showed no emission. The gate voltage causes electrons to be continuously tunnelling from the inverted substrate to the gate. When these electrons are injected into the conduction band of the SiO_2 excite Si-nc, generating electron-hole pairs that recombine radiatively[3, 4, 17]. The spectrum is centred at ∼725 nm and has a full-width at half-maximum of ∼220 nm. Compared to bulk silicon, this represents a ∼0.6 eV of gap expansion as a consequence of quantum confinement, which corresponds[18] to a

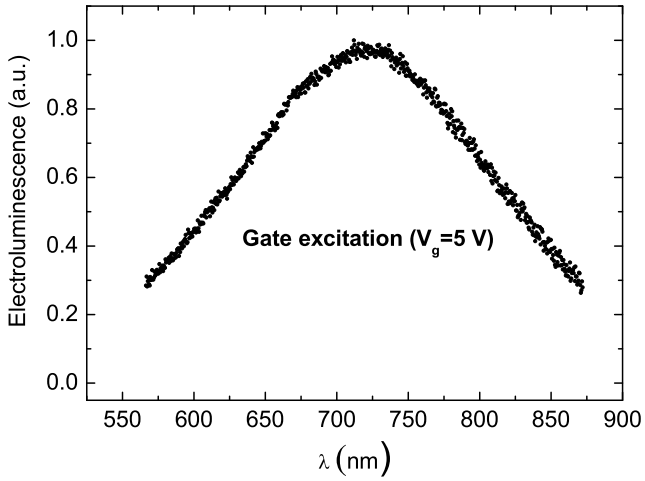

Figure 2. Silicon nanocrystal emission spectrum under gate 5 V_{DC} electrical excitation. Light emission is due to exciton recombination in the array, caused by impact excitation of electrons from the inverted channel.

population of excited Si-nc with an average size of 4-5 nm. This observation is in agreement with particle sizes measured by EFTEM.

3.2. Modulation by suppression of the Fowler-Nordheim gate excitation

Time-resolved EL (figure 3) is measured in response to a square wave (amplitude of 5V) applied to the gate and is well fitted by a stretched exponential function[19] with τ=2 μs (β=0.6). The EL peak observed each time the gate voltage is abruptly switched from negative (positive) to positive (negative) bias is attributed to a combination of i) sequential exciton formation by injection of electrons (holes) from the inversion (accumulation) layer[14, 20] and ii) impact excitation of carriers of different type[4, 17]. After $\sim$20 μs, the signal reaches its steady state; the device works with DC current flowing between the electrodes and shows a continuous EL (reduced by $\sim$50% from its initial peak value), attributed to impact excitation of electrons injected from the inversion layer. Electroluminescence modulation from an alternating current (AC) gate voltage beyond a few kHz is not possible because it is inherently limited by three known mechanisms[4, 14]: carrier tunnelling times, Si-nc radiative lifetimes and gate capacitance time constant. Although there is some room for improvement regarding injection times and capacitive delays by engineering device geometrical features and dielectrics, nothing can be done up to now to significantly change radiative lifetimes of Si-nc as dramatically as it would be required. Under AC gate excitation, the maximum frequency for which EL modulation is observed in our transistors is about 50 kHz. As shown in figure 4, at 100 kHz there is a strong loss of the two states that define the digital modulation, and only sharp peaks are observed at the gate voltage transitions. At even higher frequencies such as 500 kHz, a frequency corresponding to the inverse of Si-nc radiative lifetime, not only the modulation states are lost, but also the optical

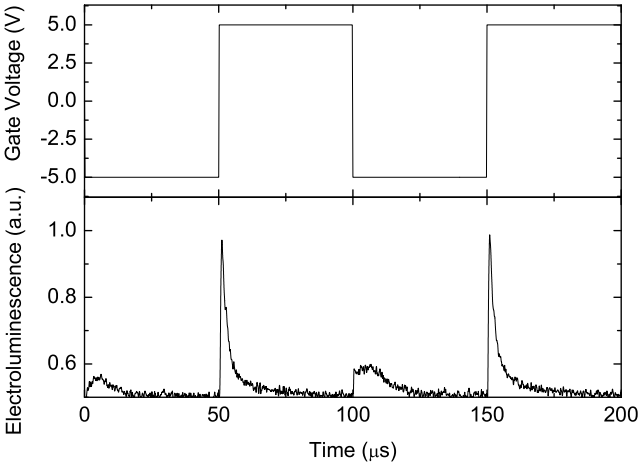

Figure 3. Time-resolved electroluminescence under AC gate excitation. A stretched exponential fits the observed decay. Note the important contribution of the DC electroluminescence offset (50% of the peak value) .

signal drops to zero. This results confirm[4] that AC gate modulation cannot exceed the kHz-range, completely dissipating any chance of applicability. An interesting complete study of the frequency response of AC gate excitation may be found in reference[14].

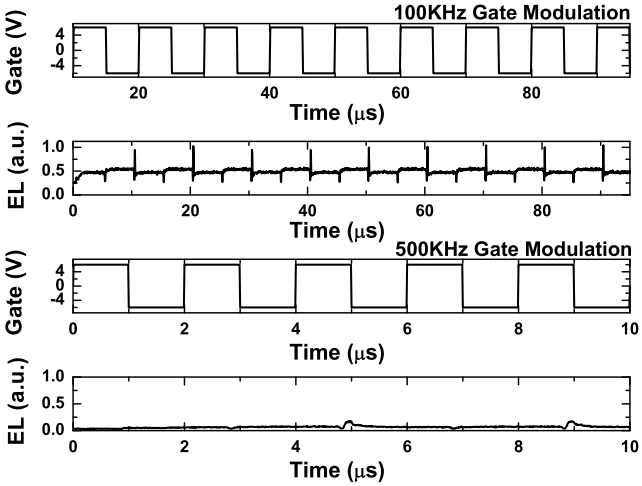

Figure 4. AC gate modulation. At 100 kHz, the gate voltage discontinuities can be detected in the electroluminescence. At 500 kHz the electroluminescence signal drops to zero.

3.3. Modulation by Channel Hot Electron injection of the continuous Fowler-Nordheim gate emission

The slow AC gate capabilities demonstrated in the preceding section have to do with the fact that the electrical excitation has to be switched on/off each time a bit of information is encoded in the optical signal. The other possibility we consider here is making use of independent fields; one is applied across the gate structure in DC and is the responsible

of Si-nc excitation and thus electroluminescence, whilst the other is applied along the channel in AC, generating a controlled injection to/from Si-nc that results in EL fast de-excitation/excitation. The physical mechanism responsible of this fast de-excitation is the Auger effect, which plays an important role once Si-nc have been charged with an excess of carriers. As reported elsewhere[21, 22], the Auger de-excitation timescale is in the range from ps to ns, so the modulation speeds attainable by using this approach may reside in the GHz to THz range. The mechanism responsible of the Si-nc charge

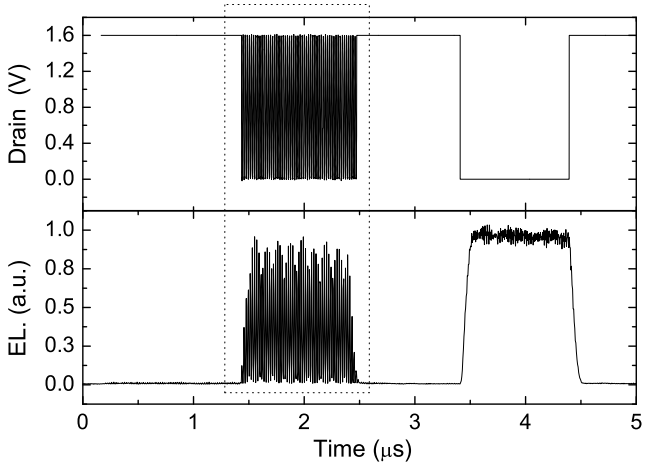

Figure 5. 5 V_{DC} gate excitation along with 1.6 V_{AC} drain modulation.

injection is channel hot electron (CHE). Nowadays, this mechanism is widely used to program commercial NOR-type Flash memories, and it is known to allow a fast injection and induce higher threshold voltage shifts (roughly proportional to the charge present in the dielectric) than a FN programming[23]. A constant gate voltage above threshold ($V_G > V_{th}$) causes light emission from nanocrystal excitons. When a positive voltage is applied to the drain ($V_D < V_G$), an electric field along the channel is created, which accelerates electrons from source to drain. The shape of the energy of electrons in the channel has been extensively studied in the literature and is usually described by a heated non-Maxwellian energy distribution[24] with a pronounced energy tail close to the drain. Thanks to this raising of average energy and due to an increased lateral velocity (parallel to the Si/SiO_2 interface), the injection of electrons into the Si-nc layer is dramatically improved while the number of electrons arriving to the gate is decreased, as will be demonstrated in the electrical characterization section later on.

Upon this increase in the density of electrons throughout the Si-nc layer, the conditions are optimized for Auger relaxation to take place, which in turn results in EL suppression. While a Si-nc is charged, electro-excitation of an additional electron-hole pair is still allowed due to the high density of excited states. However, in this charged state, the energy involved in the excitonic recombination is more efficiently transferred to the additional charge carrier already present in the nanocrystal, resulting in no net photon emission.

Figure 5 shows the observed modulation through drain cycling while the gate is

fixed at 5V. Effective EL suppression is observed when the nanocrystal layer is flooded with electrons through CHE. The EL signal is rapidly detected once the drain voltage is grounded; the excess of electrons is now swept out by the gate voltage to the gate and effective FN impact ionization is recovered. Thus, we get rid of the most limiting factors of gate modulation. First, since the modulating signal is applied along a MOSFET channel in inversion, capacitive charging time constant is negligible. Secondly, because EL suppression by Auger processes is a sub-nanosecond non-radiative path, modulation of Si-nc emission is achieved at rates several orders of magnitude faster than the (μs-range) Si-nc population radiative decay times. Leaving aside Auger recombination, the speed performance of a device working through this principle would be ultimately limited by both the ability to inject/remove charge to/from the electroluminescent centres and the transistor (drain-to-source) frequency response (bandwidth).

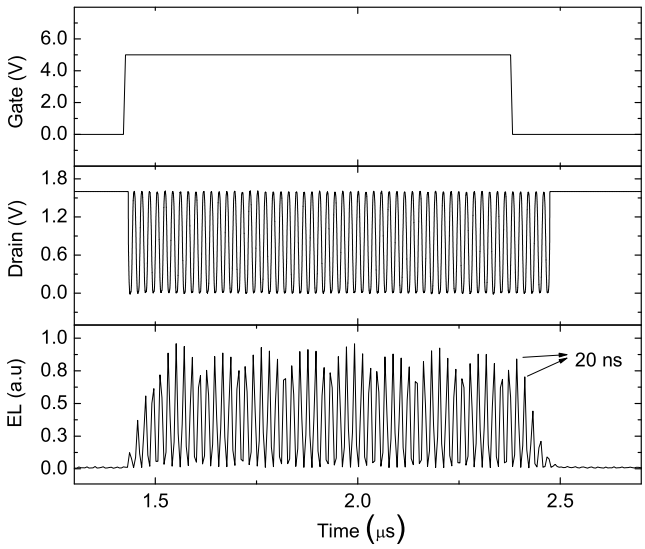

Figure 6. Detail of AC drain modulation. Electroluminescence is quenched at positive drain cycles.

Figure 6 shows a detail of the modulated signal. Although the period of the electrical signal is 20 ns, the full-width at half-maximum of the drain pulses is 10 ns (at this high frequencies the drain signal is not a square wave but sinusoid-like), corresponding to a 100 MHz. The time resolution of our photon-counting system is 5 ns, and no higher frequencies could be tested in this work because of the equipment limitation. This lack of resolution under 100 MHz drain excitation explains the small amplitude oscillations observed in the optical signal, as a poor number of counts within the 5 ns time-bins cause statistical variations. This artefact is considerably smoother at 50 MHz. It is also worth noting that once the gate DC excitation is switched off, the solely application of the AC drain signal is able to modulate the light decay for a few nanoseconds more, as there still remain some excitons who have not yet recombined. This decay has not necessarily to have the same time constant as that of gate modulation in figure 3 due to the fact that now is affected by the drain signal, which consumes

excitons non-radiatively at positive semi-cycles, giving rise to a decreased time constant.

The modulation depth (MD, defined as the ratio between the amplitude of the modulated signal and the constant optical signal level before modulation) is the figure of merit of optical modulators. In order to determine the influence that the drain signal has in the MD, a set of square waves differing in their positive/negative values (V_{high} and V_{low}) are sequentially applied to the drain terminal, while the gate is biased at 5V. Time-resolved EL is measured on the same device for each waveform maintaining the same integration time and detector sensitivity. For each (V_{high},V_{low}) pair, the MD is plotted in figure 7. A MD of about 95% is obtained for (V_{high},V_{low}) =(1, 0) V, indicating that drain voltages well below the gate bias are required to efficiently inject electrons through the thin tunnel oxide. For V_{low}=0 V and V_{high} >1 V, pinch-off of the channel occurs and drain current no longer depends on drain voltage, which is manifested as a saturation of the MD. Although source and drain in a MOSFET are symmetrical terminals, V_{high} and V_{low} are not completely interchangeable as a high (negative) V_{low} significantly increases the electric field in the oxide and strongly contributes to impact excitation from the drain region. When V_{high}=0 V and V_{low} >-2 V, MD is still acceptable (80%) but rapidly decrease for V_{low} <-2 V, as a pinched-off channel cannot compensate the strong voltage dependence of a FN drain injection. It should be noted that MDs higher than 100% are measured for (V_{high} , $|V_{low}|$)> (2, 2) V , again attributed to a suppression of signal while V_{high} is applied, and an impact excitation enhancement or amplification taking place at V_{low} as a consequence of an increased effective oxide field . Although the latter regime of operation may be prone to device wear-out, we do not observe any sign of degradation under continuous operation over weeks.

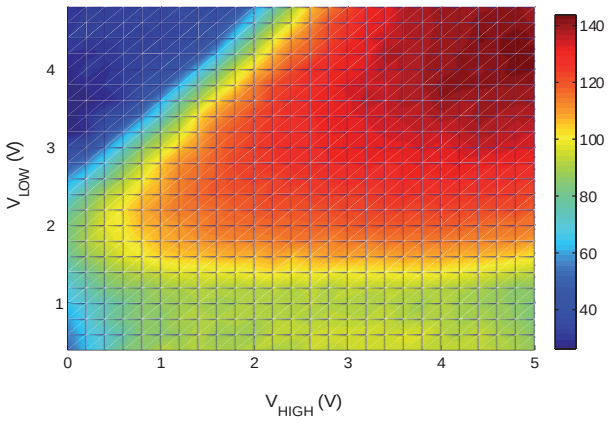

Figure 7. Modulation depth for different positive/negative values of the square waves applied to the drain.

4. Electrical properties. FN versus combined FN+CHE.

To begin with, standard transistors that have not suffered a Si^+ ion implantation are studied. The gate area of these transistors is 22×30 μm^2. The conductance method is used to determine the fresh V_{th} (threshold voltage) of the transistors from the I_d-V_d (drain current versus drain voltage) plot. By this method, the V_{th} is defined as the voltage point where the tangent of the I_d-V_d curve (at the point where the channel conductance peaks) intercepts the line I_d=0 A. As can be seen in figure 8, the application of this method gives V_{th}=1.1 V, a typical value for an NMOS transistor.

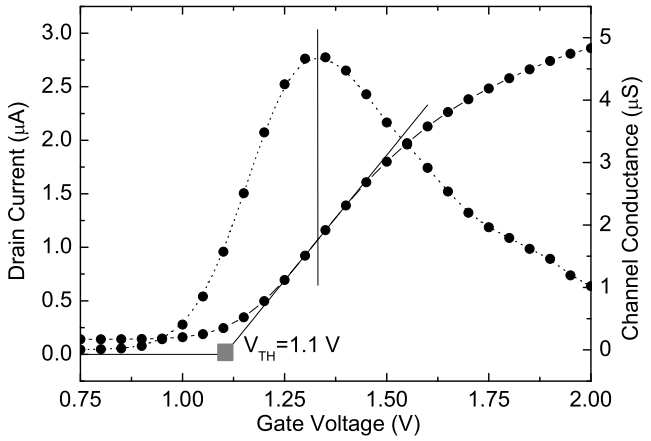

Figure 8. Drain current (solid) and channel conductance (dotted) as a function of the gate voltage. A V_{th} of 1.1 V is extracted from the tangent line at the conductance peak.

For a thick enough oxide (pure SiO_2 without Si-nc or defects), the dominant current mechanism is of FN type[25]. This mechanism takes place when the applied gate voltage raises the Fermi level so that carriers see a triangular potential barrier instead of a trapezoidal shape. Although, theoretically, this always happens at 3.1-3.2 eV for pure SiO_2, practically, FN currents can only be observed at high fields (they are in the sub-fA range at low-medium fields for thick oxides). The FN current expression reads,

$$I = A_{eff}\frac{q^2 m_o}{8\pi h m^*_{ox}\Phi_b}\frac{V^2_{ox}}{T^2_{ox}}\cdot exp(-\frac{8\pi\sqrt{2qm^*_{ox}}T_{ox}\Phi_b^{3/2}}{3hV_{ox}}) \quad (1)$$

where V_{ox} is the oxide voltage, q, the electron charge, h, the Planck's constant, m_{ox}/m_o=0.5 the effective mass of electrons in the SiO_2 conduction band, Φ_b, the injection barrier height, and A_{eff}, the effective emission area at the injecting electrode.

Figure 9 shows multiple I_g-V_g (gate current versus gate voltage) plots for different V_d's (drain voltages). The dotted traces correspond to fitted curves to experimental data through the FN formula. For V_d=0 V, an oxide thickness of T_{ox}=14.8 nm is extracted from the fit (by maintaining fixed the device area A and the electron's effective mass m_{ox} to its known value). Although the FN expression does not take into account the heating of carriers in the channel when a drain voltage is applied (in fact, it makes use of

a Fermi distribution at zero temperature for both contacts), it can be used to estimate the effect of a drain voltage, in terms of an increased or decreased effective barrier Φ_b that electrons have to surmount to tunnel to the gate. For $V_d \neq 0$, Φ_b is left as a free parameter while A=6.6×10^{-6} cm^2 and T_{ox}=14.8 nm are fixed. The inset of figure 9

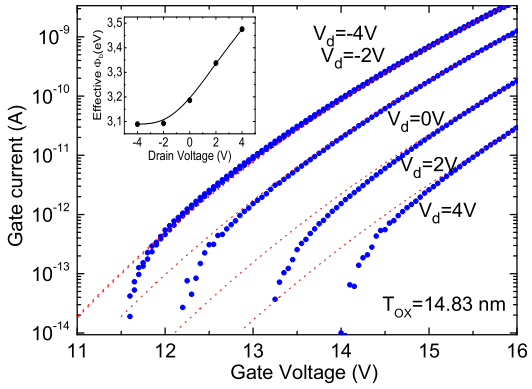

Figure 9. $I_g - V_g$ plot for transistors with pure SiO_2 gate oxides. Dotted curves are fitted data to the Fowler-Nordheim tunnelling expression. The inset shows the effect of drain voltage on the Si/SiO_2 barrier extracted from the fitting.

shows that the extracted value of Φ_b coincides with that reported for Si/SiO_2 (3.1-3.2 eV) only for $V_d \leq 0$ but linearly increases for $Vd > 0$. Since the gate voltage is positive, this can be attributed to a decrease of the gate oxide electric field as a consequence of the applied (positive) drain voltage, which in turn reduces the gate current. It can also be concluded that CHE injection to the gate does not play any role for such a thick-oxide without Si-nc. This can be explained by noting that the voltage applied to the gate is much higher than that applied to the drain. Carriers impinge the SiO_2 interface at high frequencies and the effect of the weak drain-to-source field is not enough to change the carrier's velocity along the channel. A drain voltage of 4 V is translated into a small increase of the effective Φ_b for tunnelling from 3.2 eV to 3.5 eV as a consequence of an oxide field reduction.

Figure 10 shows a comparison between I_d-V_d curves for reference and Si-nc samples. Both transistors clearly show characteristic ohmic and saturation regions. However, it should be noted that transistors with embedded Si-nc in the gate oxide have an earlier onset of saturation, and once it is reached, it takes place at a lower drain current value. This is the first signature of nanocrystal charging. The drain current starts saturating at V_d=V_g-V_{th} to a drain current that linearly depends on $(V_g$-$V_{th})^2$. While for the reference sample V_{th} is independent of V_g, this is not the case for transistors with Si-nc in the gate oxide. When a gate voltage is applied, charge is injected from the substrate to the Si-nc layer which increases V_{th} and in turn reduces the quantity (V_g-V_{th}) so that the onset and value of saturation are linearly and quadratically diminished respectively.

A second evidence of nanocrystal charging can be found in the I_d-V_g hysteresis

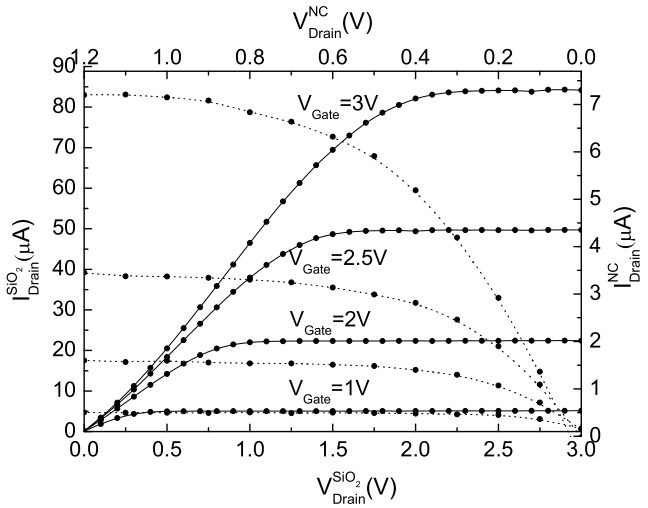

Figure 10. I_d-V_d curves for reference transistors (solid) and transistors with embedded Silicon nanocrystals (dotted) for different gate voltages.

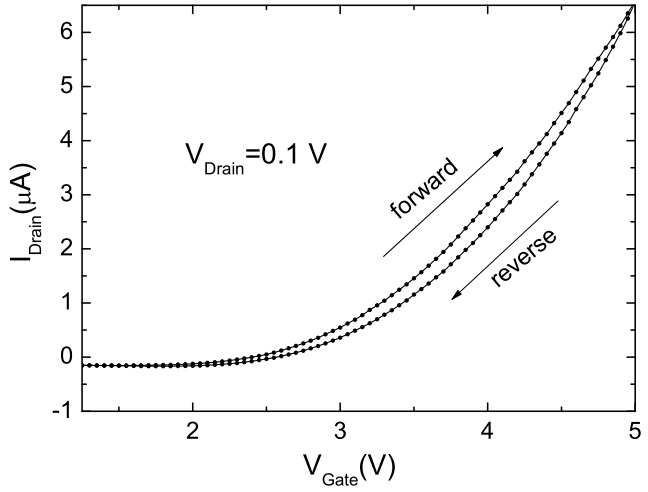

Figure 11. I_d-V_g reversible hysteresis curve attributed to charge trapping in the nanocrystals.

(figure 11). During the forward gate voltage sweep, nanocrystals are charged with electrons from the inverted channel. Since the charge density in the oxide is increased, the gate voltage must be higher in order to compensate the charge screening from electrons from Si-nc and create an inversion layer in the channel. When the reverse sweep is performed, the threshold voltage is now higher than it was at the forward sweep, giving rise to a lower drain current as a consequence of a drop in the channel conductance.

Gate current through SiO_2 with embedded nanoparticles can be detected at gate voltages as low as 1-2 V in contrast to the 11-12 V required for reference samples. As shown in figure 12, the gate current is decreased with increasing drain voltages, which is not only attributed to a lowering of the oxide field but, in this case, also to a repulsive

field created as a consequence of a charging of the nanocrystals, as will be seen later on.

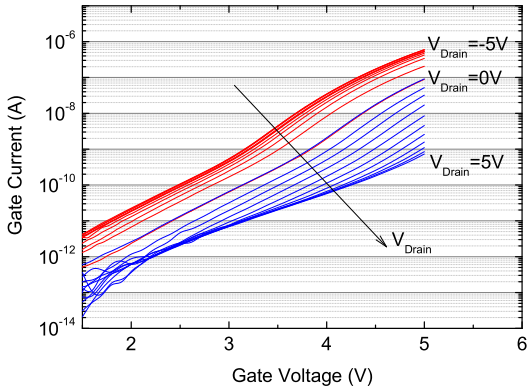

Figure 12. Effect of negative and positive drain voltages on I_g-V_g for nanocrystal transistors.

The transport mechanisms along oxides with embedded nanoparticles at low fields are quite complicated, and so far, all models have given unsatisfactory explanations of the processes involved, limiting to experimental fits of data to semi-empirical expressions such as FN, Direct Tunnelling (DT), Poole-Frenkel (PF), or trap-assisted tunnelling (TAT), among others, depending on the voltage range and temperature. However, what is generally true, is that at high fields, the FN behaviour is recovered as long as a pure oxide region exists. This can be easily understood by considering that at low electric fields, the effect of the relatively low inter-nanoparticle tunnel transparencies involved may be considerable and measurable, but at higher fields, the carriers tunnel with ease until reaching the pure SiO_2 interface, which becomes the most limiting interface to overcome. Thus, at high fields, although oxides with Si-nc are orders of magnitude more conductive, the functional dependence is still of FN-type, but with a reduced oxide thickness T_{ox} and area of conduction A. The reduced thickness corresponds to the thickest region that comprises a pure oxide region, and the conduction area may be different as the number of nanocrystals that form the gate current bottleneck may vary.

Recent studies[26] performed on similar MOSFETs with low-energy implanted Si^+ have evaluated the CHE injection compared to FN. It is found that CHE charging not only is more efficient concerning programming windows (threshold voltage shifts or charge stored in the Si-nc layer) but also are more reliable. Our device has been under continuous operation (V_g=5 V (DC) and V_d=1 V (AC)) for approximately 200 hours (6×10^{12} drain cycles), without exhibiting any sign of degradation in terms of either luminescence intensity or threshold voltage instabilities.

The effectiveness of the CHE mechanism to inject charge into the Si-nc layer is studied in figures 13 and 14 for negative and positive drain voltages respectively.

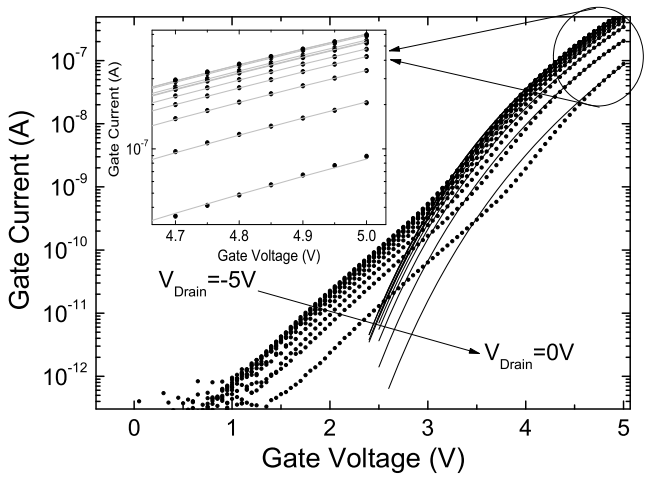

Figure 13. I_g-V_g curves for negative drain voltages. Solid lines correspond to Fowler-Nordheim fitted data. The inset shows a close up of the high field region.

The FN expression can be satisfactorily used to fit data for negative drain voltages, giving the expected barrier height Φ_b=3-3.2 eV for the Si/SiO_2 interface. However, as mentioned before, the effective oxide thickness and area of conduction significantly decrease compared to reference samples. From the fitting, a T_{ox} ∼2 nm and an area A=1.2×10^{-11} cm^2 are inferred. Since the ion implantation distribution peak of the Si^+ ions is located at ∼10.5 nm from the gate electrode (as confirmed by EFTEM micrograph in figure 1b), nucleation of Si-nc at 2 nm from the gate must be very unlike to occur. Assuming that the probability of finding a Si-nc at 2 nm from the gate contact can be calculated through the ratio of effective areas of conduction for Si-nc and reference samples, one gets a probability of P(2 nm)=1.2×10^{-11}/6.6×10^{-6}=1.6×10^{-6}, that is, at most a couple of Si-nc over a million are located at 2 nm from the gate. At typical Si-nc densities of 10^{12} Si-nc/cm^2, this means that only ∼10 nanocrystals are driving the gate current. In the less favourable casenvisagede (V_g=5 V and V_d=-5 V) and for an average nanocrystal of 4-5 nm in diameter, this implies a current density through the 2 nm-thick oxide of 10^4-10^5 A/cm^2. This high current densities are easily achieved in thin-oxide transistors[27]. However, as drain voltages of V_d=1 V are sufficient to get 100% modulation depths, operational current densities for the 2 nm-thick oxide drop to 100 A/cm^2. It should be noted that these current densities are related to the current flowing through the nanocrystal bottleneck but the gate current density is only about 0.01 A/cm^2.

The value deduced for the probability of finding a Si-nc at 2 nm from the gate can be further supported by assuming a Gaussian distribution of nanocrystals along the oxide. As the mean value of this distribution obtained by EFTEM is ∼10.5 nm and assuming a probability of 1.6×10^{-6}, the standard deviation is calculated to be 2.6 nm, which is compatible with the EFTEM micrograph that shows a self-aligned single layer of Si-nc, with no appreciable dispersion.

Figure 14 shows the experimental data along with the corresponding FN fitted

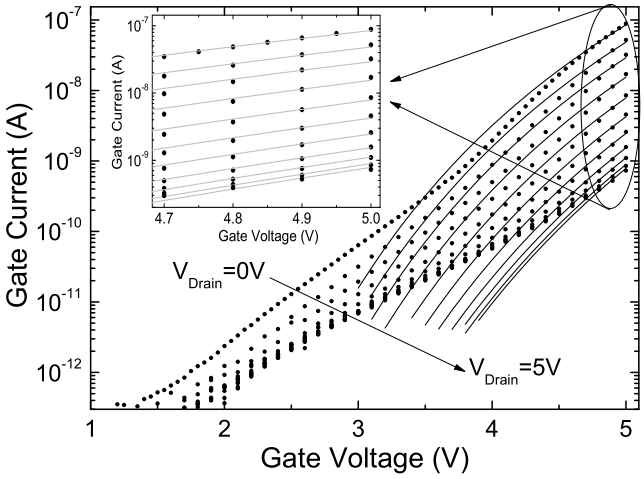

Figure 14. I_g-V_g curves for positive drain voltages. Solid lines correspond to Fowler-Nordheim fitted data. The inset shows a close up of the high field region.

curves for positive drain voltages. In this case, using the same parameters as for the fitted curves of figure 13, the goodness of the fittings is slightly degraded, specially at gate voltages considerably smaller than 5 V, indicating a change of conduction mechanism from FN to CHE as V_d increases. A Φ_b versus V_d plot (as shown in figure 15) gives a Φ_b in the range of 3-3.2 eV for negative drain voltages, as also found in control transistors. In contrast, for V_d above 0 V, the Φ_b increase is much more pronounced than in references samples. While in reference samples the increasing of Φ_b was attributed to a lowering of the oxide field caused by the drain voltage, in the sample with embedded Si-nc, Φ_b is even further increased as a consequence of a repulsive screening of the charge injected into the Si-nc. This is a direct evidence of the high efficiency of CHE injection because i) it reduces the FN impact excitation gate current by diverting charge to the nanocrystal layer, thus improving reliability, ii) the reduction is not primarily caused by a lowering of the field oxide due to the drain positive voltage (as for reference samples), but by the electrostatic repulsion of electrons already injected in the Si-nc layer.

5. Conclusions

In this article, we present the operation principles of a Si-nc light emitting transistor which exploits Auger relaxation to obtain modulation of electroluminescence from Si-nc at speeds at least three orders of magnitude faster than radiative recombination rates. We demonstrate that AC gate excitation is not suitable if switching speeds higher than radiative recombination rates of Si-nc are required. Instead, a new approach involving i) gate DC excitation and ii) drain AC channel hot electron injection may be used to increase the Auger coefficient. The fast Auger quenching overcomes the limitation imposed by radiative decay times, obtaining modulation rates of 200 Mb/s at modulating voltages of 1 V and modulation depths of 100%. Detailed electrical characterization of

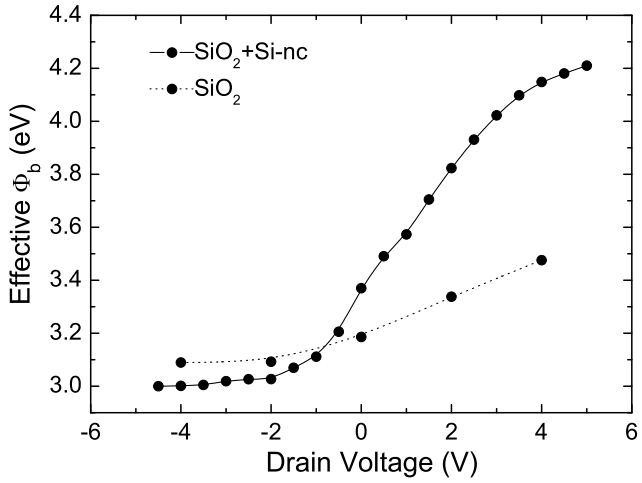

Figure 15. Comparison between the extracted electron Si/SiO_2 barrier (Φ_b) for reference (dotted) and nanocrystal transistors (solid). Electron injection into silicon nanocrystals causes an increased Φ_b attributed to an electrostatic screening.

Si-nc and control samples has been performed as a support to the optical findings. The properties and conduction mechanisms through Si-nc have been studied and used to clarify and quantify the effect of FN and CHE on the Si-nc excitation and charge trapping, coherently supporting the main ideas found optically.

Several applications can be foreseen from the principle of Auger-controlled quenching of luminescence, in topics such as biological sensing integrated into CMOS or direct encoding of information into light from Si-nc or Erbium. Much scientific effort is devoted to optimize Si-nc doped with Erbium systems, with the aim of obtaining net optical gain and eventually an integrated Silicon laser. The direct modulation principle proposed herein, could be potentially integrated in such systems, avoiding or reducing the necessity of stand-alone electro-optical modulator stages in Silicon chips. Other advantages to conventional electro-optical modulators include less current consumption (from the theoretical minimum of 10^5 A/cm^2 in nowadays Silicon electro-optical modulators to $\sim$1 A/cm^2 in our non-optimized device), and extremely low modulating voltages ($\sim$1 V for MD of 100%). As a consequence of power dissipation, one of the main problems that face silicon modulators operating through plasma dispersion effects is their poor scalability. This limitation is fully overcome with a modulator operating under a transistor approach, as the scaling capabilities of mainstream electronics technology are conveniently inherited. Although ultra-scaled transistors ensure high modulation rates, it should be pointed out that, for a single transistor, aggressive scaling could lead to low-level light detection demands integrated on-chip. This compromise between speed and optical power is easily solved through a large scale of integration on the minimum area required for detection. Although low-level luminescence from ultra-scaled MOSFETs may not seem appropriate for Silicon photonics, other interesting applications out of the scope of this work may be easily envisaged, such as the study of single photon on-demand emitters.

Acknowledgments

Josep Carreras acknowledges support for sample fabrication in the Integrated Nano and Microelectronics Clean Room at IMB-CNM through the ICTS access program from the Spanish Ministry of Science and Education.

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