Design and Implementation of an 8-Bit 1-kS/s Successive-Approximation ADC

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Abstract: Successive-approximation (SAR) analog-to-digital converters (ADCs) are among the most common and widely used general-purpose ADC architectures for their moderate resolutions and sampling rates. This paper aims to study and understand the conventional SAR ADC by proposing an N-bit architecture with a split capacitor digital-to-analog converter (DAC), and design, simulate, and finally implement a functional 8-bit 1-kS/s 0-5V SAR ADC prototype on a breadboard. The simulations and the tested prototype allow us to analyze the results and notice some of the most relevant advantages and disadvantages of the SAR ADC besides its limitations.

I. INTRODUCTION

Any physical system provides a continuous signal of the characterized magnitude. However, in an ever-growing digital world, the vast majority of computers and devices work in the digital domain since it is easier to manipulate, store and display data. The devices responsible for this processing are the data-acquisition-systems (DAS), in which analog-to-digital converters (ADCs) play a fundamental role. The processing begins when a transducer receives and transforms the magnitude of the physical phenomenon into an analog electrical signal. Once conditioned, this signal goes to an ADC, which is the electronic component in charge of discretizing it in the time domain, quantizing it, and finally converting it into binary-coded data that a digital device can process.

Overall, two parameters characterize the performance of any ADC: the bit resolution and the sampling rate. However, in eneral, if one is required, the other must be forfeited and vice versa. Even so, different ADC architectures span the entire spectrum of resolutions and sampling rates, each with unique characteristics and distinct limitations. Hence, it is essential to choose the proper ADC in terms of speed, accuracy, resolution, space or power consumption according to the application [1].

The scope of this paper is to study the successive-approximation (SAR) ADC, one of the most common architectures for its moderate-to-high resolutions (8 - 16 bits) and sampling rates (1 kS/s - 10 MS/s) besides its low-power consumption. This combination of features makes it the ideal converter for portable data acquisition systems that do not require high speeds or resolutions. Take implanted biomedical acquisition systems, such as pacemakers or cardiac defibrillators, for instance. These devices, which are implanted in the human body and used to monitor biomedical signals, tend to use this type of ADC for its low power consumption and reduced area [2], [3].

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II. PROPOSED ARCHITECTURE

The SAR ADC is a counter-type analog-to-digital converter based on a feedback loop operation resembling the Ramp ADC and the Tracking ADC. However, unlike these two, the SAR ADC has a successive approximation register that performs a binary search algorithm to estimate the value in the minimum sequence of counts within the full-scale range.

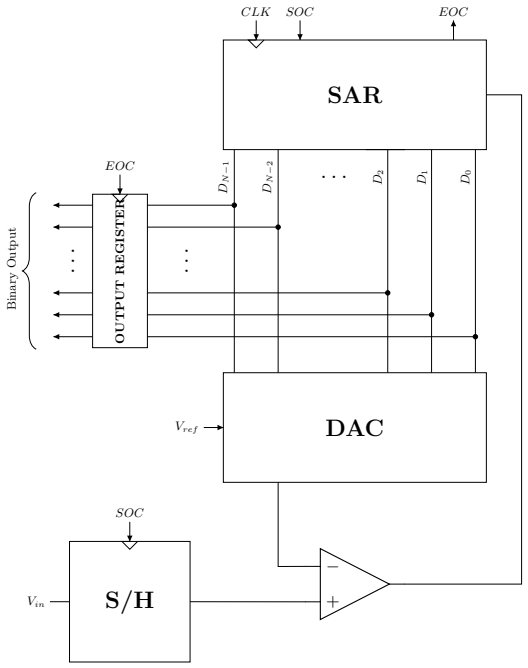

FIG. 1: Block diagram of the proposed N-bit SAR ADC architecture.

As shown in Fig.(1), the main blocks of the conventional SAR ADC comprise a sample-and-hold (S/H) circuit, a comparator, a successive-approximation-register (SAR) and a digital-to-analog converter (DAC).

The conversion begins at the S/H circuit, where the input voltage, V_{in}, is sampled, outputting an enduring value for each conversion that will act as a reference for the value to estimate. Simultaneously, an operational

amplifier (op-amp) compares whether the proposed value in the DAC is higher than the reference or not and, therefore, if the SAR logic has to clear or hold the bit during the next iterations to get closer to the reference. Once the conversion period has ended, the output register outputs only the last N bits of each conversion.

In the following subsections, each block of the proposed SAR ADC architecture is depicted in more detail.

A. Sample-and-Hold Circuit

Most ADCs have a sample-and-hold (S/H) circuit at the beginning, whose principal function is to hold the value of the analog signal until the ADC has finished processing all the information of each conversion. In some SAR ADC, the DAC has a build-in S/H circuit, which reduces the area and power consumption of the SAR [4]. However, in the proposed architecture, an explicit S/H circuit independent of the DAC is suggested.

The most elementary S/H circuit only uses a capacitor and an analog SPST switch, which toggles between the sample and hold mode at the sampling rate. The switch is closed during the sampling stage, letting the input signal pass through and charge the capacitor. When the switch opens, the capacitor is isolated from the input and holds the value until the next conversion. A voltage follower is often used at the output to avoid load effects.

B. Comparator

The purpose of the comparator is to contrast the values proposed by the SAR logic and later converted by the DAC with the constant value of the S/H circuit, which acts as a reference of the value to be estimated. As a result, the comparator generates a logic output depending on whether the proposed value is higher than the reference or not.

The comparator consists of a single op-amp with no feedback loop. Nevertheless, it is probably one of the most crucial elements of the SAR ADC, not only because it is the bridge between the analog and the digital domain but also because it limits the SAR ADC sampling frequency. As the sampling rate increases, the op-amp time to make a decision and reach saturation decreases to the point where saturation is never reached again, which results in misleading comparisons. Therefore, the maximum SAR ADC sampling rate depends on how quickly the op-amp can make unambiguous decisions.

Besides being fast, the op-amp also has to be accurate to resolve voltages within the resolution of the converter. The difference between two discrete successive values decreases as the resolution increases, $V_{LSB} = V_{ref}/2^N$. Therefore, if the op-amp cannot resolve voltages below V_{LSB}, higher resolutions will not be noticed.

To summarize, a high-performance and high-precision op-amp is required considering that the comparator acts as a bottleneck for both resolution and sampling rate, limiting the SAR ADC performance.

C. Successive-Approximation-Register

The SAR logic performs a binary search algorithm based on a feedback loop to approximate the value in the minimum sequence of comparisons between all quantization levels. As shown in Fig.(2), the algorithm begins with a start of conversion (SOC) pulse that erases all bits from the previous conversion. Subsequently, the SAR logic proposes a change in the most-significant bit (MSB), setting it to 1. Then, if the feedback value of the DAC is greater than the reference, the proposed change is accepted, increasing the feedback value by $V_{ref}/2^{N+1-n}$, where n is the bit number, and the bit remains set until the next conversion. Otherwise, the SAR refuses the change, and the bit is reset again to 0, decreasing the feedback value by $V_{ref}/2^{N+1-n}$. Once the MSB is known, the loop is repeated for the subsequent bits until it reaches the least-significant bit (LSB). When all bits have been checked, an end of conversion (EOC) control signal is set high and the algorithm starts again.

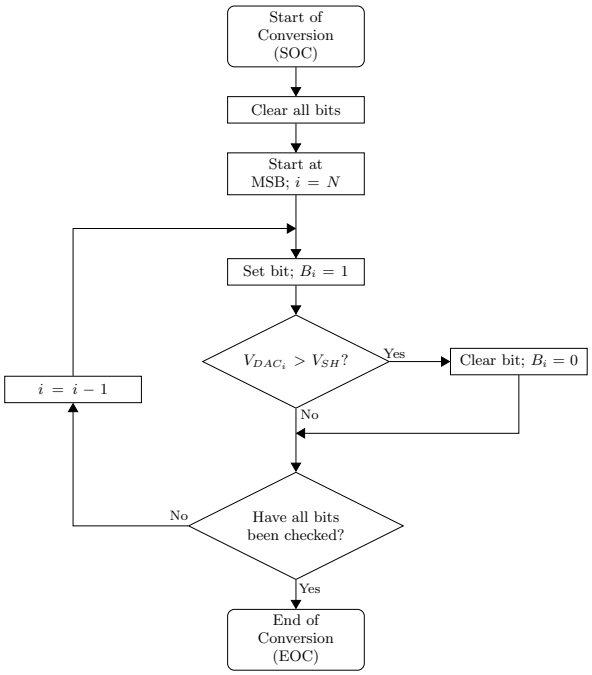

FIG. 2: Flowchart of the binary search algorithm used by the SAR logic to approximate a value.

The suggested SAR circuit is shown in Fig.(3) and is based on the one proposed in [5]. Its design comprises N+1 set-reset D flip-flops that act as a sequencer and another N set-reset D flip-flops as a code register. The sequencer shifts a 1 on each clock cycle, setting the corresponding flip-flop of the code register so that the bit and, therefore, the digital output change, proposing a

new estimation. Moreover, the succeeding flip-flop of the sequencer is used as a clock to decide if the proposed value is accepted or refused depending on the feedback of the comparator. At the end of each conversion all flip-flops are reset.

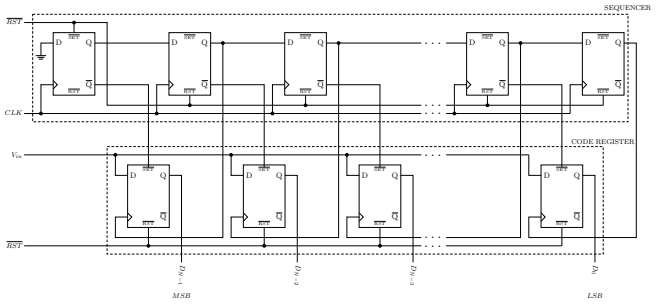

FIG. 3: Schematic of the proposed N-bit SAR logic circuit.

According to the proposed structure and algorithm, the N-bit SAR ADC lasts N+2 clock cycles to complete all the comparisons and approximate a value: N cycles to perform the binary search algorithm, one cycle to store the data and the last cycle to restart all the flip-flops. Therefore, the internal circuit frequency, f_{CLK}, has to be at least N+2 times higher than the sampling rate, f_s.

D. Charge Scaling DAC

The digital-to-analog converter is the block where digital data is converted back to analog and fed to the comparator to close the feedback loop.

The most common DAC architecture in SAR ADCs is the binary-weighted capacitor due to its low-power consumption. This architecture consists of a parallel array of N binary-weighted capacitors followed by SPDT analog switches connected to either V_{ref} or ground, depending on whether the digital input is high or low. Consequently, the output voltage will be a function of the charge in each of the capacitors and can be generalized for any digital input by Eq.(1):

$$V_{DAC} = \sum_{n=0}^{N-1} D_n 2^{N-n} V_{ref} \tag{1}$$

Where D_n is the logical value of the n^{th} digital input.

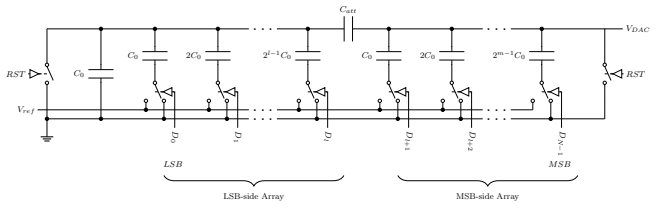

FIG. 4: Schematic of the proposed N-bit split capacitor DAC.

However, high-resolution binary-weighted DACs require high-value capacitors, so in this case, in order to reduce their values a slight variation was suggested. The architecture proposed is the split capacitor DAC, which adds an attenuation capacitor to split the array into an LSB-side array and an MSB-side array, as shown in Fig.(4). The value of the attenuation capacitor is determined by [6]:

$$C_{att} = \frac{1 + \sum_{n=0}^{l-1} 2^n}{\sum_{n=0}^{m-1} 2^n} C_0 \tag{2}$$

Where l and m are the number of capacitors in the LSB- and MSB-side arrays and C_0 is the unit capacitor.

As with the comparator, the DAC also plays a crucial role in the SAR ADC performance, especially in terms of sampling rate and resolution. On the one hand, the values of the capacitors limit the sampling rate of the SAR ADC as enough time should be left between conversions for the capacitors to charge fully. Otherwise, the comparator will decide before the voltages on the capacitors are sufficiently settled, resulting in erroneous decisions. On the other hand, the capacitor mismatch is one of the principal sources of non-linearities in the DAC, limiting the SAR ADC accuracy and resolution [7].

E. Output Register

The output register is the last block of the SAR ADC, and its functionality is to take the last bits of each conversion and output them since those will be the closest to the input signal. The output register consists of N parallel D-type flip-flops with a common clock running at the sampling rate, f_s.

III. SIMULATION RESULTS

To simulate the circuit we used a high-performance Simulation Program with Integrated Circuit Emphasis (SPICE) software called LTSpice®. Although it is not explicitly designed for logic circuit simulations, it also incorporates, to a lesser extent, some digital behavioral models that will suffice for the simulations proposed in this paper. The aim of the simulations was to test the performance of an 8-bit SAR ADC within the range of 0-5V using the architecture proposed in section II.

We wanted the simulations to be as close to reality as possible since we intended to implement a real prototype. For this reason, we tried to simplify the circuit as much as we could, using the minimum number of voltage sources. The analog components were polarized between ±15V, while the comparator and the digital components were polarized between 0 and +5V. Furthermore, the +5V voltage source was also used as V_{ref} in the DAC, causing the dynamic range of the SAR ADC to be between

0 and 5V. Also, a variable frequency square signal was used as a clock. Finally, in order to analyze the results, we digitalized a 0-5V 10Hz sinusoidal signal, as shown in Fig.(5).

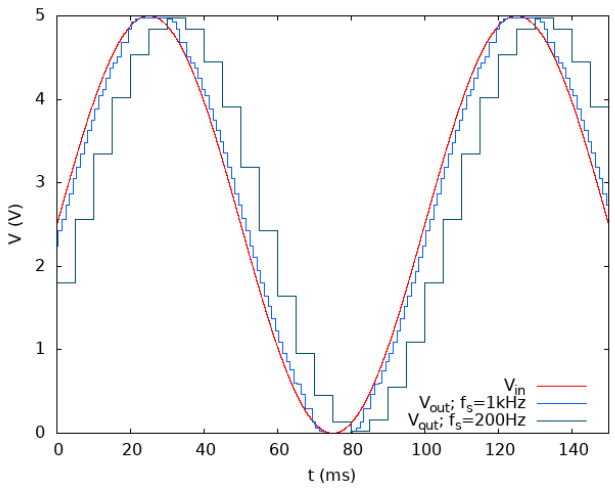

FIG. 5: Simulation of the digitalization of a 0-5V 10Hz sinusoidal signal with the proposed 8-bit SAR ADC at different sampling rates.

The best way to analyze the performance and linearity of any ADC is through its transfer curve, which shows the output of the ADC for each possible input. This type of plot presents the non-linearities of a real ADC, and therefore, a thorough analysis of the potential error sources can be performed.

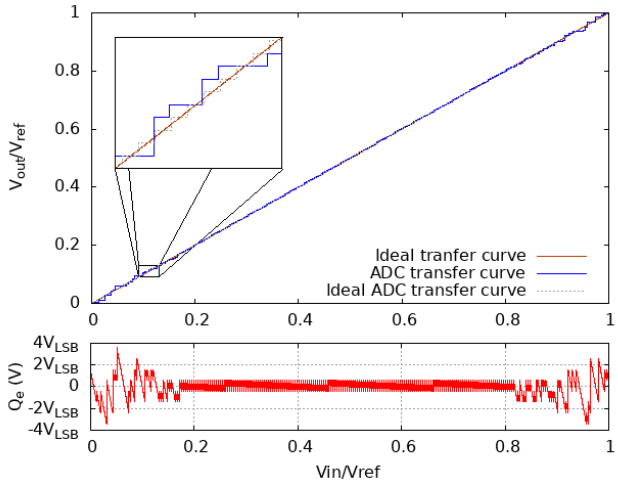

FIG. 6: Transfer curve and quantization error, Q_e, of the proposed 8-bit SAR ADC architecture.

In Fig.(5), at first sight, several discrepancies can be noted between the analog signal, V_{in}, and the digitalized ones, V_{out}. Apart from the fact that V_{in} is continuous, whereas V_{out} is discrete, a shift between both signals appears. This shift is due to the nature of the SAR ADC, as it requires a specific amount of time to perform the binary search algorithm. As shown in Fig.(5), the higher the sampling rate, the smaller the delay.

As we can see in Fig.(6), an intrinsic error appears due to the quantization. This error is known as quantization error, Q_e, and is inherent to each ADC regardless of the type. Ideally, Q_e is a zero-centered sawtooth waveform no greater than $\frac{1}{2}V_{LSB}$. In Fig.(6), we can see that Q_e differs slightly from the ideal one when quantizing voltages near zero and V_{ref}, resulting in non-linearities and ultimately in missing codes, as it can be seen in the transfer curve and the Q_e in Fig.(6) and the peaks and valleys of the sinusoidal signal in Fig.(5). The responsible for these errors is the op-amp used as a comparator (LT1001 [8]) and its polarization. Although the op-amp is polarized between 0 and 5 V, the effective input range is less than that, in our case between 0.9 and 4.1 V. Consequently, the op-amp could not compare voltages below 0.9V and above 4.1V correctly. This error could be fixed using a different type of op-amp or polarizing the comparator between -1 and 6V. However, as we did not have another op-amp model and we wanted to use the minimum number of voltage sources, the error was neglected considering that it only affected the edges of the SAR ADC performance and the fact that it was below $4V_{LSB}$.

During the simulation process, we could observe that, as mentioned in section II, the principal limitations of the SAR ADC performance are the comparator and the DAC, especially in terms of sampling speed and resolution. As far as the sampling rate is concerned, the simulations allowed us to determine that the maximum speed of the designed SAR ADC was 1kHz since, for higher sampling rates, the comparator could not follow the system. In our case, the converter was not affected by settling problems since the capacitors of the DAC, $C_0 = 5nF$, were carefully selected according to the maximum sampling frequency set for the converter. As for the resolution, the comparator was a high-precision op-amp [8] capable of resolving voltages below V_{LSB}. Therefore, the accuracy of the ADC was mainly limited by the capacitor mismatch in the split capacitor DAC considering that to maintain a proper scaling between the LSB- and the MSB-side array, the attenuation capacitor had to have a fractional value according to Eq.(2). Given that this fractional value is complicated to meet, it was approximated by $C_{att} \simeq C_0$, affecting the overall accuracy of the SAR ADC.

IV. IMPLEMENTATION OF A SAR ADC

Finally, based on the proposed architecture and using the simulations as a guide, an 8-bit 1-kS/s 0-5V SAR ADC was implemented in a breadboard, as shown in Fig.(7).

In order to check the proper performance of the SAR ADC, a 1-4V 10Hz sinusoidal signal was digitalized at a sampling rate of 100Hz. The result was checked in an

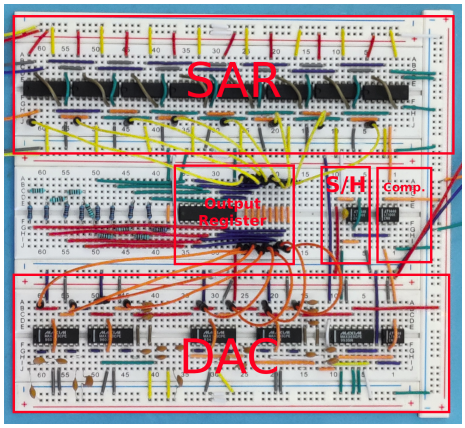

FIG. 7: 8-bit 1-kS/s 0-5V SAR ADC prototype implemented on a breadboard.

oscilloscope, as shown in Fig.(8).

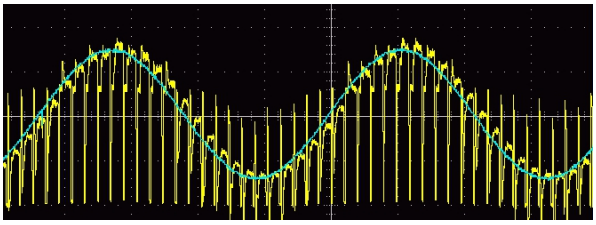

FIG. 8: Digitalization of a 1-4V 10Hz sinusoidal input signal (blue) with the implemented 8-bit 1-kS/s SAR ADC and the output of the DAC (yellow). The subdivisions in the x axis corresponds to 25ms and the y axis to 1V.

In Fig.(8), the expected results of the output of the DAC can be observed and contrasted with the simulations. The voltage of the sampled signal was set between 1-4V since, according to Fig.(6), the best performance of the ADC is in this range. Also, as discussed in the simulations, we observed that for frequencies above 1kHz the system could not digitalize the signal due to the low speed of the comparator.

V. CONCLUSIONS

We have successfully achieved the implementation of a functional 8-bit 0-5V 1-kS/s SAR ADC and digitalized an analog signal with it, as shown in Fig.(8). Furthermore, we have been able to characterize the linearity and performance of the designed SAR ADC through simulations and face some of its typical errors and limitations, which helped us understand the behavior of the SAR ADC in depth. On the one hand, we have seen in both the simulations and the implementation that the op-amp used as a comparator acts as a bottleneck for the sampling rate, not resolving frequencies above 1 kHz and this being the maximum frequency of the SAR ADC. This limitation has forced us to work in sampling rates lower than the usual ones in this type of ADC. On the other hand, the capacitor mismatch in the split capacitor DAC attenuation bridge will limit the resolution and accuracy of the system. Once we have obtained insight into the SAR ADC behavior, future work may focus on improving its performance, such as increasing the sampling speed or resolution and also correcting errors.

Acknowledgments

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[1] S. Bashir, S. Ali, S. Ahmed and V. Kakkar, "Analog-to-digital converters: A comparative study and performance analysis," 2016 International Conference on Computing, Communication and Automation (ICCCA), Noida, 2016, pp. 999-1001, doi: 10.1109/CCAA.2016.7813861.

[2] G. Huang, S. Chang, C. Liu and Y. Lin, "A 1-µW 10-bit 200-kS/s SAR ADC With a Bypass Window for Biomedical Applications," in IEEE Journal of Solid-State Circuits, vol. 47, no. 11, pp. 2783-2795, Nov. 2012, doi: 10.1109/JSSC.2012.2217635.

[3] D. Zhang, A. Bhide and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13-μm CMOS for Medical Implant Devices," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1585-1593, July 2012, doi: 10.1109/JSSC.2012.2191209.

[4] S. R. Nitnaware, A. D. Tijare and M. M. Matey, "Design of binary architecture for Successive Approximation Analog-to-Digital Converter," 2015 International Conference on Communications and Signal Processing (ICCSP), Melmaruvathur, 2015, pp. 0512-0516, doi: 10.1109/ICCSP.2015.7322537.

[5] T. Anderson, "Optimum control logic for successive approximation A/D converters", Comput. Des., pp. 81-86, July 1972.

[6] R. J. Baker, "Data Converter Architectures" in CMOS: Circuit Design, Layout, and Simulation, 1st ed., Wiley, 1997, ch. 29, sec. 1.5, pp. 805-810.

[7] C. Huang, H. Ting and S. Chang, "Analysis of Nonideal Behaviors Based on INL/DNL Plots for SAR ADCs," in IEEE Transactions on Instrumentation and Measurement, vol. 65, no. 8, pp. 1804-1817, Aug. 2016, doi: 10.1109/TIM.2016.2562198.

[8] Linear Technology. "LT1001: Precision Operational Amplifier Data Sheet". LT1001 datasheet, rev. B. Accessed: Feb. 2, 2021. [Online]. Available: `https://www.analog.com/media/en/technical-documentation/data-sheets/LT1001.pdf`