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Effect of Si_3N_4 Mediated Inversion Layer on the Electroluminescence Properties of Silicon Nanocrystal Superlattices

Julian López-Vidrier, Sebastian Gutsch, Oriol Blázquez, Jan Valenta, Daniel Hiller, Jan Laube, Javier Blanco-Portals, Lluís López-Conesa, Sònia Estradé, Francesca Peiró, Blas Garrido, Sergi Hernández and Margit Zacharias*

Dr. J. López-Vidrier, Dr. S. Gutsch, Dr. D. Hiller, Dr. J. Laube, Prof. M. Zacharias,
Laboratory of Nanotechnology, IMTEK, Faculty of Engineering, Albert-Ludwigs Universität Freiburg
Georges-Köhler-Allee 103, 79110 Freiburg (Germany)
julia.lopez.vidrier@imtek.uni-freiburg.de
O. Blázquez, Dr. L. López-Conesa, J. Blanco-Portals, Dr. S. Hernández, Dr. S. Estradé, Prof. F. Peiró, Prof. B. Garrido
MIND-IN^{2}UB, Departament d'Enginyeries: Electrònica, Universitat de Barcelona
C/ Martí i Franquès 1, 08028 Barcelona (Spain)
Prof. J. Valenta
Faculty of Mathematics and Physics, Charles University
Ke Karlovu 3, 121 16 Prague 2 (Czechia)
Dr. L. López-Conesa
Unitat TEM-MAT, Centres Científics i Tecnològics de la Universitat de Barcelona (CCiTUB)
Lluís Solé i Sabarís 1, 08028 Barcelona (Spain)

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Abstract

The achievement of an efficient all-Si electrically-pumped light emitter is a major milestone in present optoelectronics still to be fulfilled. Silicon nanocrystals (Si NCs) are an attractive material which, by means of the quantum confinement effect, allow attaining engineered-band gap visible emission from Si by controlling the NC size. In this work, SiO_2-embedded Si NCs are employed as an active layer within a light-emitting device structure. We demonstrate that the use of an additional thin Si_3N_4 interlayer within the metal-insulator-semiconductor device design induces an enhanced minority carrier injection from the substrate, which in turn increases the efficiency of sequential carrier injection under pulsed electrical excitation. This results in a substantial increase of the electroluminescence efficiency of the device. Here, the

effect of this Si_3N_4 interlayer on the structural, optical, electrical and electro-optical properties of a Si NC-based light emitter is reported, and the physics underlying these results is discussed.

1. Introduction

Given the huge impact of quantum confinement on the electronic properties of silicon nanocrystals (Si NCs), namely the band structure modification as a function of the NC size,[1–4] in-depth studies have been carried out on the physical mechanisms involved in the optical[5–7] and electrical[8–10] performance of SiO_2-embedded Si NCs, and their potential to become active material candidates in optoelectronic applications such as light-emitting devices (LEDs).[11–13] Light emission from Si NCs has recently become a very promising field, which can set a basis for novel fully-Si based optoelectronics and photonics. Indeed, the photoluminescence (PL) quantum yield (QY) of Si NCs in SiO_2, i.e., the ratio between the photons that are absorbed in and emitted from Si NCs, has been estimated by several groups, and QY efficiencies exceeding even 30% have been reported.[14,15] Nevertheless, the case of electron-to-photon conversion is not so straightforward in SiO_2-embedded Si NCs, because carrier injection is strongly limited by the high band offset between the Si NC and the dielectric host, which can only be overcome under certain tunnelling conditions.[16] In this respect, some works have addressed the excitation mechanisms that govern the electroluminescence (EL) emitted by size-controlled Si NCs in SiO_2. Among the most accepted hypotheses, electron-hole pairs are believed to be formed within Si NCs after bipolar carrier injection and/or impact ionization via high-kinetic energy electrons; whereas the former approach claims that electrons and holes are injected from the electrodes to the NC system at a similar rate,[17,18] the latter takes into account the asymmetry of injection efficiency due to the mobility difference between both carriers in the oxide.[19,20] In any case, the overall power efficiency of these systems, i.e., the ratio between the optical output and the electrical input, is low.

Aiming to increase the power efficiency of Si NCs/SiO_2-based light emitting devices, different strategies have been conceived. Such is the case of the pulsed electrical excitation of Si NCs-based LEDs, which was found to substantially enhance their EL emission yield by more than one order of magnitude, apart from reducing device degradation and power consumption.[21–26] This approach takes advantage of the sequential carrier injection within the NCs, which improves the poor bipolar injection efficiency shown by hot carrier-based conventional DC excitation mechanisms. In particular, the work by Walters *et al.* reported a metal-oxide-

semiconductor field-effect transistor (MOSFET) structure. Here, the channel created between the heavily-doped drain and source terminals acts as a selective carrier injection layer that allows for "charge-programming" the Si NCs embedded in a bulk SiO_2 layer, with holes in accumulation and electrons in inversion, as illustrated in **Figure 1a** and **Figure 1b**, respectively.[21,22] The key point of this device design takes place in inversion conditions, where an *n*-type channel is created between drain and source that provides additional electrons to the substrate ones. In another approach, Creazzo *et al.* opted for a MOS capacitor structure, much simpler in terms of design than a transistor device, where the active oxide material consisted of several Si NC superlattices.[26] Learning from these structures, we propose here an alternative NC-based device design that allows for an improved sequential injection while preserving the simplicity of the MOS design. Specifically, we employ the intrinsically high positive charge density of Si_3N_4,[27] which we place between the Si substrate and the NC-based active layer. In substrate accumulation conditions (**Figure 1c**), holes from the substrate are normally accumulated at the substrate/interlayer interface, thus being injected into the NC-based layer. The real advantage of this structure is found in substrate inversion regime, where a permanent inversion layer underneath the interlayer region surrounding the gate contact can supply large amounts of electrons for the region underneath the gate. This structure mimics Walter's *n*-type MOSFET channel by injecting additional electrons from the substrate into the NCs (**Figure 1d**). Therefore, this interlayer is expected to enhance the injection of both carriers into the NC-based active layer under the corresponding polarization regimes.

We will demonstrate here that the controlled generation of an inversion layer through the above described interlayer approach results in a significant enhancement of the EL efficiency of Si NC-based MOS capacitors under pulsed electrical excitation. For this, we designed three different samples allowing us to compare the obtained results not only with our previous works but also with those reported in the literature. With this objective, a careful structural, optical, electrical and electro-optical characterization is carried out, from which the carrier injection and Si NC excitation mechanisms that take place within our devices can be assessed. It is the aim of this work to study in detail the effect of the hereby selected different device configurations on the EL performance of Si NC-based LEDs.

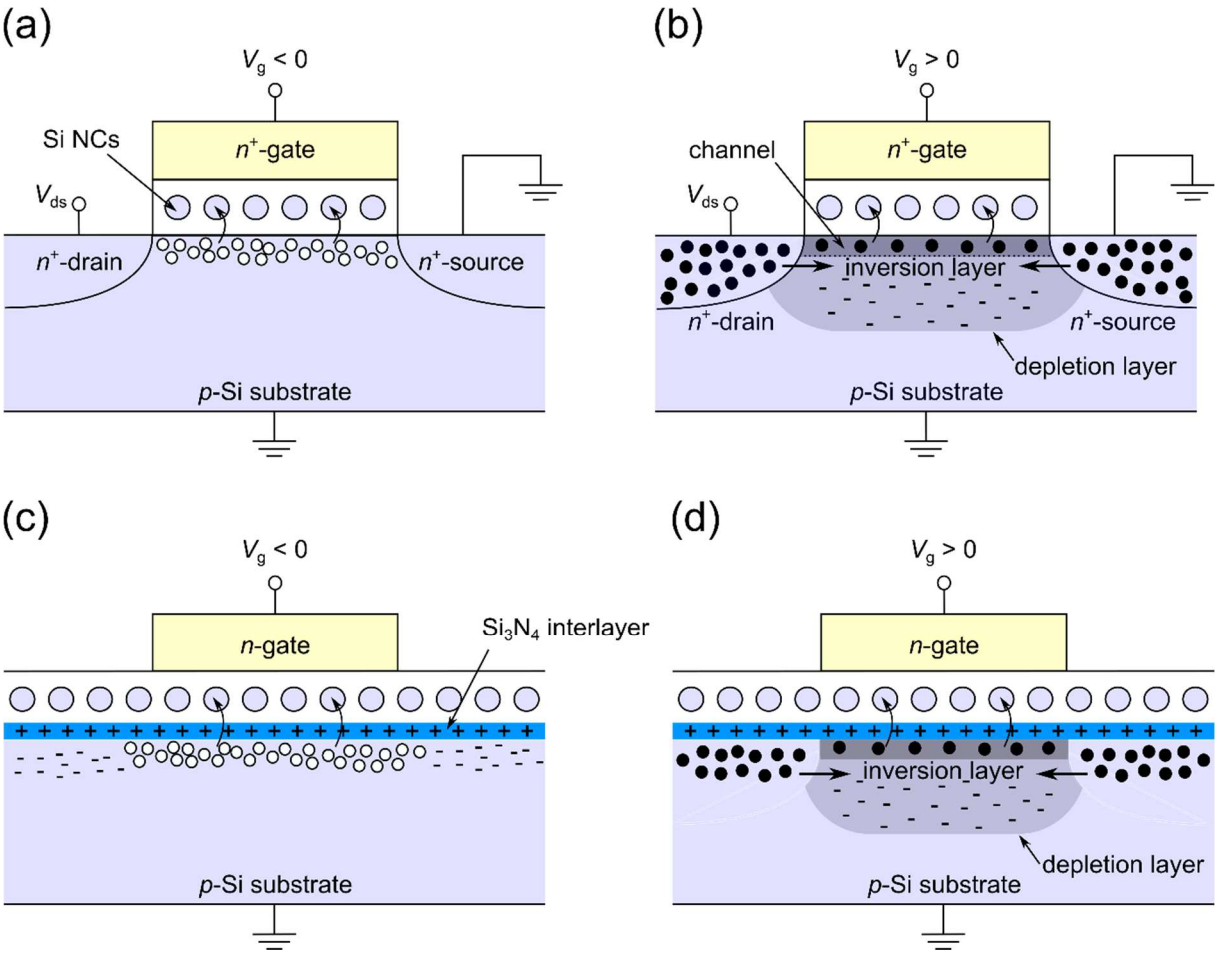

Figure 1. Cross-section schematic of the Si NC-based MOSFET device employed by Walters *et al.*, adapted from Ref. [21], in either substrate (a) accumulation or (b) inversion regimes, where sequential carrier injection from the substrate, respectively holes (open circles) and electrons (full circles), is fostered. V_{ds} and V_g are, respectively, the drain-source and gate voltages. (c) and (d) display the sketch corresponding to the proposed MOS device design that includes an intrinsically-high positively-charged interlayer (in blue), respectively in substrate accumulation and inversion regimes. Such an interlayer will present fixed positive charges (+), whereas fixed negative charges (-) are present within the substrate. The shaded regions in (b) and (d) indicate the inversion layer (dark grey) and depletion zone (light grey) formed below the NC-based layer.

2. Results

2.1. Material Structure Inspection

The employed approach makes use of an engineered inversion layer, which allows tuning the carrier injection mechanism into the Si NCs and, as a result, allows modifying their EL emission in a controlled manner. To inspect this effect, three different samples were fabricated. The basic structure (labeled as *NC*) contains a stack of 5× Si NC/SiO_2 superlattices (SLs, nominal layer

thicknesses of 4.5 nm and 1 nm, respectively, total active layer nominal thickness of 27.5 nm) deposited on top of a *p*-type Si substrate. This number of SLs was selected according to general EL performance criteria, since thicker SL stacks exhibit poor carrier injection (and thus higher EL onset voltage) and thinner ones release a barely observable luminescence. Top and bottom contacts were made by transparent and intrinsically-conductive (*n*-type) ZnO and Al contacts, respectively. The inversion layer is achieved by the inclusion of a 2 nm Si_3N_4 interlayer between the Si substrate and the first Si NC/SiO_2 bilayer, which constitutes the device labeled as *NC-SN* (total nominal thickness of 29.5 nm). This interlayer thickness was found to be optimum for our investigation purposes, since slightly thicker layers do not affect the superlattices PL, whereas they clearly decrease the current density through the device. Finally, the additional effect of blocking the carrier injection from the top electrode is analyzed by embedding a 10 nm SiO_2 layer between the last NC layer and the ALD-ZnO top electrode, in the device labeled as *NC-SN-SO* (total nominal thickness of 39.5 nm). In **Figure 2**, the schematics corresponding to the three device designs are displayed.

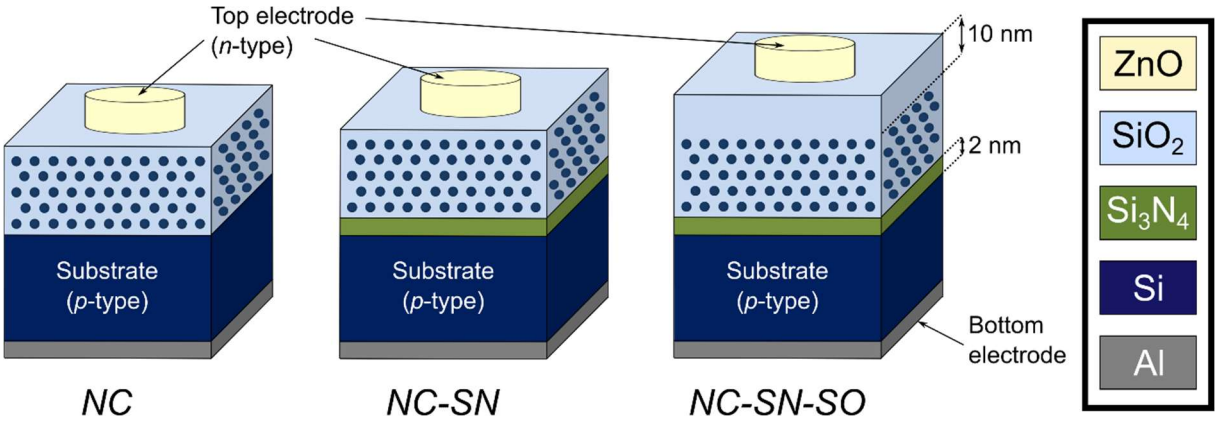

Figure 2. Sketch of the device structures under study. They essentially consist of 5× SRON/SiO_2 superlattices deposited on top of *p*-type Si substrate, with a circular ALD-ZnO top electrode and a backside full-area Al metallization (device *NC*). Device *NC-SN* contains an extra 2 nm Si_3N_4 interlayer between the Si substrate and the Si NC SLs. Device *NC-SN-SO* was designed as device *NC-SN*, but containing an additional 10 nm SiO_2 layer between the Si NC SLs and the top ZnO electrode. On the right-hand side, a legend is provided with the color correspondence to each material. Thicknesses are not to scale.

The cross-section of the devices was directly imaged by means of transmission electron microscopy (TEM). In particular, **Figure 3a** displays an energy-filtered TEM (EFTEM) image from the cross-section of device *NC-SN-SO*. This particular sample was selected since it

presents all the distinct characteristics under study, namely the Si NC/SiO_2 SLs, the Si_3N_4 interlayer and the additional SiO_2 capping layer. By filtering around the Si plasmon energy (E_{Si} ~ 16.7 eV), the contrast of the regions containing high Si content is highlighted (bright regions). This analysis allows the observation of the Si NCs, properly arranged in five ordered layers conveniently separated by ~1 nm lower-Si content barriers (i.e., the SiO_2 layers), with a total stack thickness of ~30 nm (from the substrate to the last Si NC layer). This microscopy observation is consistent with cross-section Si NCs sizes around ~4 nm, as previously reported on equivalent samples.[28,29] In addition, a ~9 nm layer is found between the Si NC superlattices and the ALD-ZnO gate electrode which, because of its identical contrast to the inter-NC barriers in EFTEM images filtering around the SiO_2 plasmon energy (image not presented), must be also composed by SiO_2. EFTEM imaging, however, gives no clear evidence of the presence of a nitride layer between the Si substrate and the Si NC SLs, which is due to the proximity between the plasmon energies of SiO_2 (~22.5 eV) and Si_3N_4 (~23.7 eV).[30] This drawback is solved by unfiltered bright-field TEM (BFTEM), as shown in **Figure 3b**, where the brightness contrast allows observing a ~2 nm layer on top of the crystalline Si substrate, which can be attributed to the Si_3N_4 interlayer.

PL spectra were acquired from each sample, whose results are displayed in **Figure 3c**. All samples exhibit a Gaussian-like spectrum ranging from 600 nm to 1150 nm. This kind of emission is typically ascribed to the radiative excitonic recombination within the Si NCs, with a full-width at half-maximum (FWHM) of ~160–170 nm observed for all samples, attributed to the NC size distribution and phonon contributions due to the indirect transition.[31] The PL emission peaks around ~940–945 nm for samples *NC* and *NC-SN*, whereas it is slightly redshifted (~965 nm) for sample *NC-SN-SO*. The occurrence of a small PL shift to longer wavelength in sample *NC-SN-SO* is likely to be caused by a modulation effect of the SiO_2 capping layer on the spectral emission properties of the Si NCs because of the internal distribution of the optical excitation field, affecting in turn the PL emission intensity.[32,33] It is interesting to note that, within the uncertainty attributed to measurement reproducibility and surface homogeneity, samples *NC* and *NC-SN* yield a virtually identical emission spectrum, which indicates that the 2 nm Si_3N_4 interlayer does not play a relevant role in the PL properties of the sample.

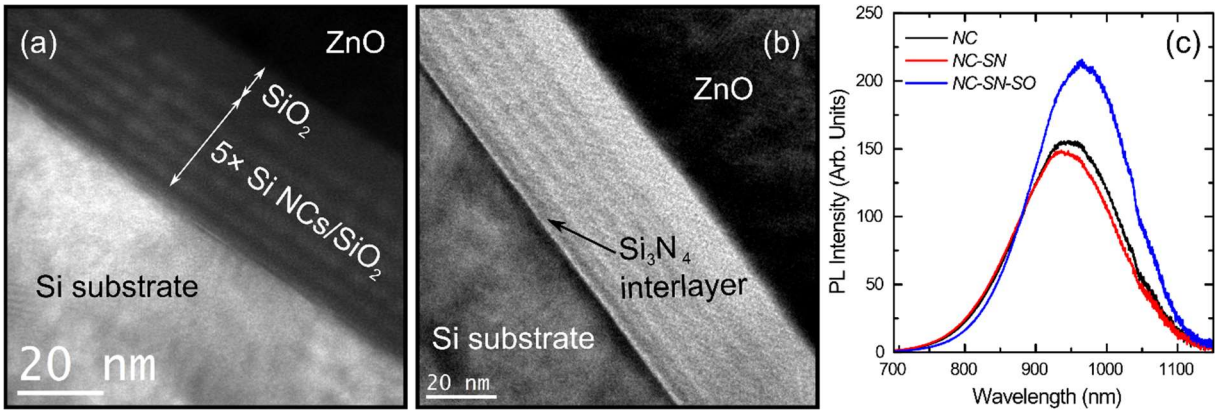

Figure 3. a) Energy-filtered and b) unfiltered bright-field transmission electron microscopy images from the cross-section of device *NC-SN-SO*. The different observed layers are highlighted. c) Photoluminescence spectra corresponding to the three samples under study.

2.2. Electrical Characterization

Figure 4a displays the current density versus electric field [$J(E)$, both in absolute values] characteristics corresponding to the three devices under study in accumulation regime, i.e., under negative applied voltage on the top ALD-ZnO electrode. Indeed, these curves already state a signature for each device structure. In particular, device *NC* shows an increase of current density of several orders of magnitude, as expected from continuous charge transport within NC-related states and no blocking layer impeding charge injection through the electrodes.[20,34] Device *NC-SN* exhibits an analogous trend to device *NC*, which reveals similar carrier injection conditions. However, in this case the curve is clearly shifted to higher voltages, which can be attributed to the fixed charges induced by the Si_3N_4 interlayer because of its highly defective nature.[27] The $J(E)$ curve corresponding to device *NC-SN-SO* presents, in contrast to the other devices, an almost flat region at low and medium electric fields. Within this electric field regime, the current is transient and governed by charge injection.[35] The current is purely capacitive as no charge traverses the SiO_2 blocking layer. At higher electric fields, persistent Fowler-Nordheim injection becomes the dominating charge transport mechanism.[34]

The electrical characterization of the devices under study was complemented by the investigation of the capacitance versus voltage [$C(V)$] curves, obtained at 300 kHz in a fast +6 V to -6 V sweep, which are plotted in **Figure 4b**. Device *NC* presents the typical behavior expected from Si NC SLs,[34] showing a flat band voltage, $V_{FB,NC} \sim$ -0.3 V, as well as the generation of a depletion region at slightly positive voltages, always exhibiting a marked difference between charge accumulation ($V < 0$) and inversion ($V > 0$) regimes. The overall capacitance value in accumulation is low (~120 nF cm^{-2}), which is attributed to the high

conductivity of the Si NC SLs under fast AC excitation. Addition of the thin nitride layer (device *NC-SN*) increases the observed capacitance (~140 nF cm^{-2}) due to a lower AC conductivity, and leads to a notably lower flat-band voltage ($V_{FB,NC\text{-}SN}$~ -2.0 V) due to the positive fixed charges within the Si_3N_4 interlayer. The effect is similar to the recently reported work by Tondini *et al.*,[36] where non-passivated defective field oxide provides a similar threshold voltage shift. Finally, device *NC-SN-SO* (with the largest capacitance, ~143 nF cm^{-2}, due to the presence of the oxide blocking barrier) also exhibits a negative threshold voltage shift. The V_{FB} decrease for this device with respect to device *NC-SN* is due to the presence of the blocking oxide, thus indicating that the effect of the fixed positive charge is reduced.

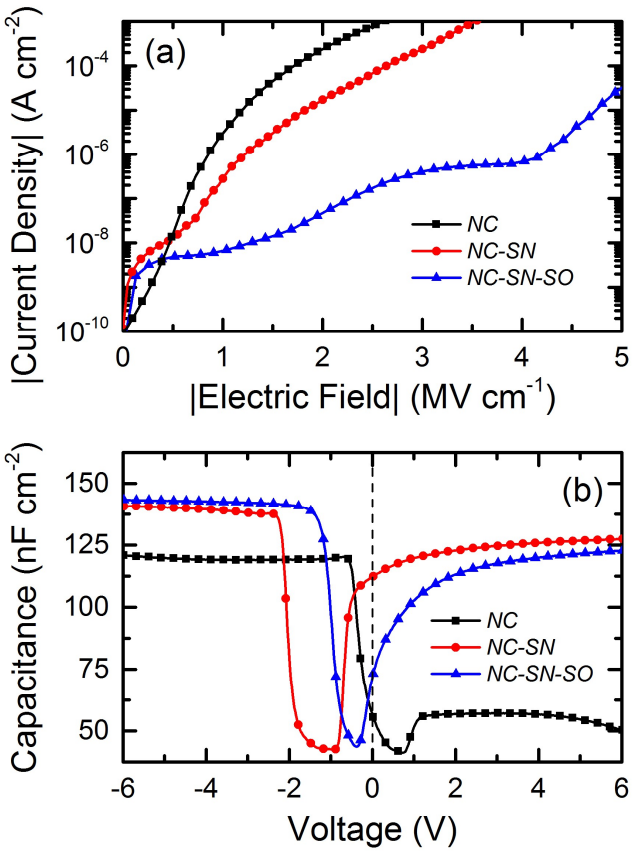

Figure 4. a) Current density versus electric field curves (both in absolute value) obtained from the three devices under study in accumulation regime. b) Capacitance versus voltage curves corresponding to the same devices.

2.3. Electroluminescence Emission

The electrical properties have shown so far that an introduced thin Si_3N_4 layer into the NC-based LED provides an inversion layer underneath the whole superlattice structure. Therefore, minority carriers are provided to the active region from the inverted areas around the gate. This

is expected to have a notable impact in the EL generation within our devices. In **Figure 5a**, the EL spectra corresponding to devices *NC* and *NC-SN* obtained under DC electrical excitation at -5 V and -10 V are displayed. In this regime, defect-induced field-ionization between neighboring Si NCs already takes place in both devices.[34] The current density of device *NC* is about one order of magnitude higher than in device *NC-SN*, which might be the reason for not observing the EL emission of the latter at -5 V. With -10 V DC excitation (~|3.4|–|3.6| MV cm^{-1}), however, the EL signal from both devices could be observed. Indeed, under these conditions, the EL emission yield corresponding to device *NC* is larger than when the Si_3N_4 interlayer is present. Also, since this voltage corresponds to an electric field (~|2.5| MV cm^{-1}) well within the blocked region of device *NC-SN-SO*, no emission was observed from this latter device.

The spectral lineshape of the EL of the devices can also be analyzed. As can be observed, devices *NC* and *NC-SN* exhibit a clear emission at low energies, within the 600–1000 nm range. When comparing these spectra with the plotted PL in **Figure 3c**, we can attribute the low-energy part of the EL spectra to the excitonic recombination within Si NCs, as has been reported before.[37,38] However, the increase in width of EL spectra ($FWHM_{NC}$ ~ 230 nm, $FWHM_{NC\text{-}SN}$ ~ 250 nm) with respect to PL can be understood as follows: smaller NC sizes are excited more efficiently via carrier injection (compared to PL, where the absorption cross-section decreases rapidly with decreasing NC size),[37,39] thus broadening the spectra towards higher energies. Please note that, although quantum-confined Stark effect (i.e., the effective reduction of the Si NC band gap, and therefore a peak redshift, due to the presence of an external electric field)[40] could also take part in our NC-based devices, our observations indicate that excitation of the small NCs population dominates the EL behavior. In the case of device *NC-SN-SO*, no EL was observed before the onset of the permanent Fowler-Nordheim current at significantly higher electric fields, as was already expected for this device. Finally, it is interesting to note that, under DC excitation, the presence of the Si_3N_4 interlayer is clearly reducing the carrier injection and NC excitation within the SLs, which results in a decreased EL emission.

Following the main aim of this work, i.e., to improve the EL emission under pulsed excitation, we measured EL with an excitation of square pulses of ±5 V, thus keeping the same amplitude as for DC excitation measurements. We used a period of 50 µs and a duty cycle of 50%, which implies accumulation and inversion times of, respectively, $t_{acc} = t_{inv} = 25$ µs (the respective results are displayed in **Figure 5b**). Please note that, for the sake of comparison, we had to apply ±8 V to device *NC-SN-SO*, which corresponds to an electric field equivalent to the one in devices *NC* and *NC-SN*, due to the additional SiO_2 blocking barrier. The most immediate result from this approach is the enhanced EL intensity in all devices with respect to DC

excitation, even when a similar voltage difference of |10| V was applied. Such an excitation scheme was first reported for MOSFET devices by Walters *et al.*,[21] and it was attributed to the sequential injection of carriers after alternate polarization switching. The enhancement is also significant for our MOS-based devices containing the Si_3N_4 interlayer, *NC-SN* and *NC-SN-SO*, with respect to the *NC* device: the EL signal has doubled, reversing the situation that was observed under DC excitation (**Figure 5b**). This demonstrates that the nitride interlayer plays a decisive role on the sequential injection and excitation mechanisms that take place under pulsed excitation.

It can also be observed from **Figure 5b** that the *NC* and *NC-SN* devices exhibit a narrower emission in pulsed than under DC excitation conditions, and centered at lower energies (in respect to NC quantum confinement-related PL emission). In our previous work, we reported on the modulation of the high- and low-energy EL emission contributions on an analogous device to *NC*, showing that shorter t_{acc} induces a high-energy (defects-related) emission quenching, which was ascribed to the insufficient time for efficient hole injection from the Si substrate into the SLs and thus the ALD-ZnO gate.[41] Additionally, we observe a narrowing ($FWHM_{NC} \sim 200$ nm, $FWHM_{NC\text{-}SN} \sim 220$ nm, $FWHM_{NC\text{-}SN\text{-}SO} \sim 220$ nm) and redshift of the EL emission in **Figure 5b** with respect to the DC excitation in **Figure 5a**. Nevertheless, these spectra still exhibit a peak blueshift and broadening with respect to the PL spectra displayed in **Figure 3c**, which confirms that the excitation of smaller NCs still prevails.

At this point, it is worth analyzing in more detail the total luminescence output from the samples. For this, the EL power efficiency (PE) of devices *NC* and *NC-SN* was estimated by exciting them with square pulses of ±5 V, using a pulse period of 80 µs and a duty cycle of 40% (which yielded the most efficient integrated EL), and collecting the whole EL emission in a 10-cm-diameter integrating sphere. The reader is kindly directed to Ref. [42] for further details on the experimental equipment and mathematical analysis of the outcoming luminescence from the devices. For evaluating the PE, we took into account the ratio between the optical power output, P_{opt}, and the electrical power input, $I \times V$ [$PE = P_{opt}/(I \times V)$]. In the case of our device *NC*, the mentioned voltage pulse conditions led to the estimation of $PE_{NC} \sim 6 \times 10^{-3}$%, whereas the utilization of the Si_3N_4 inversion layer (i.e., device *NC-SN*) induced an emission enhancement up to $PE_{NC\text{-}SN} \sim 2.6 \times 10^{-2}$%, i.e., of a factor ~4. This result is so far the maximum efficiency reached by our Si NC-based devices.[20] Please note that the PE enhancement after Si_3N_4 inversion layer incorporation is notably larger than the one observed in the EL spectra (by a factor of roughly ~2). This occurrence is due, first, to the PE normalization by the applied voltage and current (whereas voltage was fixed at -10 V, current is different in devices *NC* and

NC-SN according to **Figure 4a**), and second, to the fact that the integrating sphere collects all EL emitted by the device, whereas a small solid angle reaches the entrance slit of the spectrometer when spectrally analyzing EL.

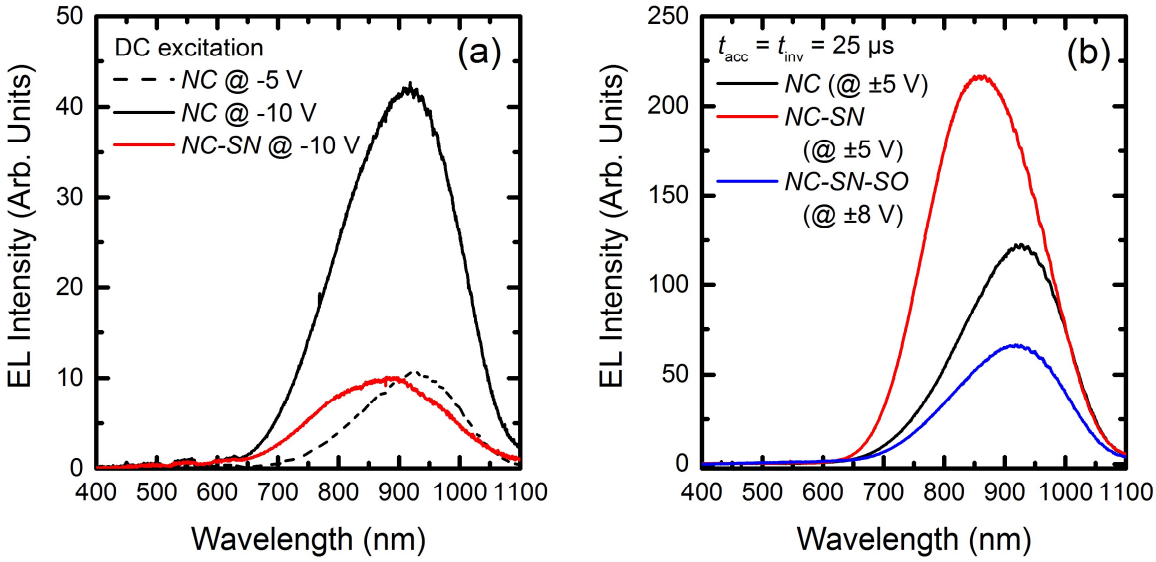

Figure 5. EL spectra corresponding to different devices, after applying (a) DC electrical excitation at -5 V on device *NC* and -10 V on both devices *NC* and *NC-SN*, and (b) 50-µs period and 50%-duty cycle square voltage pulses. The intensity scales in both graphs are directly comparable. Please note that, in (b), a higher voltage excitation at ±8 V was required for device *NC-SN-SO* in order to attain a comparable signal level to the other devices.

2.4. Recombination Dynamics and Excitation Mechanisms

The substantial enhancement of EL emission intensity from the particular device designs under study, after pulsed electrical excitation is employed, must necessarily be related to the charge injection mechanisms taking place within the devices. With the aim of understanding such injection processes, time-resolved EL studies were performed by applying controlled square voltage pulses, of ±7 V (well within the substrate accumulation and deep inversion regimes), and with a total period of 1 ms and 50% duty cycle (i.e., t_{acc} = t_{inv} = 500 µs), whose results are given in **Figure 6**. Such a long period was selected so that the whole luminescence decay, in both accumulation and inversion regimes, be complete. Again, distinct features govern the rise/decay EL pattern of the devices under test, namely the emission overshoot immediately after each polarity switch (in both polarization regimes) and the DC-like emission level reached after decay (only in accumulation). The observation of these effects is very clear in the figure.

When switching from inversion ($V > 0$) to accumulation ($V < 0$), a sudden increase in EL takes place in devices containing a Si_3N_4 interlayer (*NC-SN*), whereas device *NC* directly reaches a constant emission after switching to accumulation. Devices *NC-SN* and *NC-SN-SO* also reach a DC emission after decay from the overshoot; the device with SiO_2 blocking barrier exhibits a much lower intensity level. After switching from accumulation to inversion, an EL overshoot is observed in all devices, followed by a decay until the EL is totally quenched. Please note that the EL rise and decay times in all three devices lie in the range of 5–25 μs (rise time) and 30–75 μs (decay time), obtained by a single exponential decay fitting, which is in agreement with usual characteristic times for luminescence excitation and decay processes, respectively, taking place in Si NCs.[43–45] This indicates that we are effectively dealing with the recombination dynamics of the Si NCs/SiO_2 system, and no contribution from either the SiO_2 matrix or the ALD-ZnO electrode are observed (characterized by much faster kinetics of the order of nanoseconds).[46]

The time-resolved EL signal corresponding to device *NC* was already reported in Ref. [41] on an analogous device. In that work, the constant EL was attributed to continuous formation of electron-hole pairs within Si NCs due to bipolar injection of holes from the *p*-type substrate and electrons from the ALD-ZnO gate electrode. Because of the mobility asymmetry between electrons and holes within SiO_2,[47] some injected holes are confined in Si NCs within the layer immediately on top of the substrate which might not be recombined with electrons. During the accumulation-to-inversion switch, the positively-charged Si NCs attract electrons from the substrate until total neutralization (reaching the overshoot peak), after which EL decays. In this case, since electrons are minority carriers in the *p*-type Si substrate, no continuous electron injection is expected, because the minority carriers have to be generated thermally in the substrate. This slow process limits the current during inversion, as shown by the time-resolved current pattern (blue curves in **Figure 6**) being zero in the inversion regime.

The case of the devices containing a Si_3N_4 interlayer is different: devices *NC-SN* and *NC-SN-SO* present an additional EL overshoot after the inversion-to-accumulation switch, an effect observed in other published works in the literature, too.[21,26] As already described for device *NC*, the inversion cycle totally quenches EL emission, as expected from the complete compensation of positively-charged Si NCs with substrate-injected electrons. In this case, however, the inversion layer around the gate induced by the Si_3N_4 layer promotes additional electron supply to the SLs. The lower DC level found in device *NC-SN-SO* must be necessarily attributed to the presence of the blocking barrier. It essentially obstructs electron injection from the ALD-ZnO gate electrode. Apparently, electrons injected from the top electrode play a

decisive role in the recombination dynamics and efficiency. Finally, the difference in accumulation-to-inversion and inversion-to-accumulation EL overshoot intensity is due to the asymmetry between electron and hole Si NCs charging. As an example, in the particular case of sample *NC-SN-SO*, electron injection from the ALD-ZnO gate is strongly quenched in accumulation, which results in only hole trapping from the substrate.

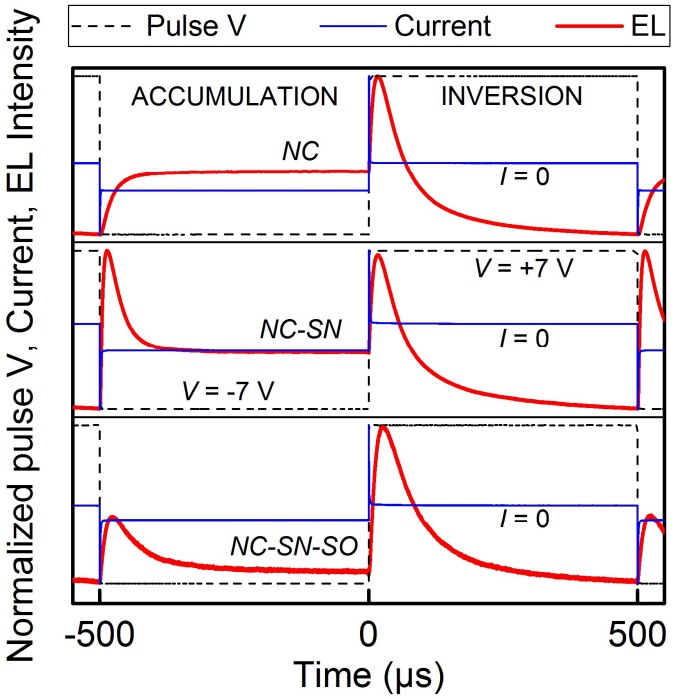

Figure 6. Normalized time-resolved EL emission (in red) from the devices under study during one voltage-pulse electrical excitation period (1 ms and 50% duty cycle). The pulse voltage (±7 V, in black dashed lines) and the current (in blue) are also indicated. For the sake of clarity, accumulation and inversion regimes are highlighted, as well as the $I = 0$ level (no current is observed in inversion).

3. Discussion

So far, numerous studies have demonstrated that the EL emission from matrix-embedded Si NCs can be strongly enhanced by means of pulsed electrical excitation.[21–23,26] This frame clearly favors the occurrence of bipolar injection being the main mechanism governing the excitation of the NCs, followed by the consequent photon emission after electron-hole pair recombination. In their work, Walters *et al.* described the sequential programming of alternately-charged Si NCs by using a field-effect transistor-like structure (a simple schematic of such structure is displayed in **Figure 1a** and **Figure 1b**).[21,22] This design presented two remarkable features: (i) the channel generated between highly *n*-doped drain and source, which

acts as an electron reservoir under alternate polarization conditions, and (ii) a SiO_2 layer between the Si NCs active layer and the poly-Si gate, which provides the adequate insulation against injection of carriers from the top electrode. Indeed, the device structure *NC-SN-SO* was intentionally designed to mimic Walters's field-effect transistor: it contains a Si_3N_4 interlayer between substrate and SLs, which has proved to act as inversion layer that provides the adjacent Si NCs with minority carriers from the substrate under alternate polarization conditions similar to case (i), plus an additional 10-nm SiO_2 blocking barrier that minimizes carrier injection from the ALD-ZnO gate, analogous to case (ii). The recombination dynamics displayed in **Figure 6** show how this device exhibits hole and electron carrier injection from the substrate immediately after switching to accumulation and inversion regimes, respectively (as demonstrated by the EL overshoots after each polarity change). In our case, however, an EL DC component is still observed in accumulation, which indicates that, at the high voltages employed (±7 V), the blocking barrier is not totally quenching the constant injection of high-kinetic energy electrons from the gate electrode.

The role of a controlled inversion layer on the bipolar injection of carriers on the Si NC-based active layer was recently studied by Tondini *et al.*.[36] They showed that the inversion layer generated after non-passivation of the field oxide surrounding the NC SLs became a source of minority electrons and holes that increased the efficiency of NC charging. This was proved by *C*(*V*) measurements, which evidenced considerable charging even under strong substrate inversion conditions, which led to a non-rectifying behavior of the overall device. Our investigations on the Si_3N_4 interlayer approach (device *NC-SN*) have corroborated these results, as can be seen in **Figure 4b**, where only device *NC* exhibits a real substrate inversion behavior, i.e., with negligible or no charging at all. In addition, both works coincide in the determination of the carrier injection nature from the inversion layer, by means of recombination dynamics studies that point out the alternated injection of electrons and holes under different polarization conditions (see **Figure 6**). In our case, absolute EL intensity measurements have shown a fourfold increase of PE in device *NC-SN* with respect to device *NC*, in excellent agreement with the enhancement shown by Tondini *et al.*. The *C*(*V*) characteristics displayed in **Figure 4b** shed light to this fact, where a clear shift of the curves towards lower V_{FB} (higher in absolute value) indicates that a similar charging level occurs at low voltages and under both accumulation and inversion regimes, which favors the sequential bipolar injection within the Si NC SLs. Despite the similar results obtained in both works, the strength of our approach lies in the simplicity of our design, where the controlled inclusion of a nitride interlayer (which has no effect on the SL structure according to **Figure 3**) provides notably higher EL emission yield from Si NCs.

Indeed, this is a very promising result, which highlights the advantages of introducing such a thin nitride layer on the performance of Si NC-based LEDs.

The EL emission efficiency of Si NC-based LEDs is limited by both carrier injection into and light extraction from the devices. In this study we have reported a maximum PE of ~2.6×10^{-2}%, which corresponds to a quantum efficiency of ~0.1% when normalizing by the number of injected electrons and the number of emitted photons (see Ref. [42] for details on this calculation). It is an interesting exercise to contextualize our result within the existing literature on the topic, where different approaches have been employed to improve either the charge injection or the light extraction issues. Perálvarez *et al.* demonstrated an EL power efficiency on SiO_2 thin film-embedded Si NCs around 10^{-3}% when grown via ion implantation, which was notably enhanced by two orders of magnitude when the PECVD technique was employed.[48] Almost simultaneously, some works on Si NC SLs were reported by Pavesi's group,[17,18] where a power efficiency as high as ~0.2% was demonstrated after DC electrical injection at low current density values.[17] In these works, however, a highly *n*-doped poly-Si gate was employed as top electrode, which notably favors tunnel-like injection of carriers within the MLs. As well, an additional 50-nm antireflective Si_3N_4 layer was employed on top of the poly-Si gate, in order to minimize optical losses.[18] In contrast, and despite its high and constant transparency throughout the visible range,[49,50] our ALD-ZnO is not optimized for light extraction. Also relevant is the achievement of external quantum efficiencies higher than 1% by means of chemically-prepared colloidal Si nanoparticles (NPs).[51,52] In these works, the colloidal Si NPs are spin-coated as emitter layer within a device structure containing polymer-based electron and hole injection and transport layers. This already states a substantial difference with respect to our SiO_2-embedded Si NCs: although the Si NC/SiO_2 superlattice structure is able to finely control the NC size, the high Si-SiO_2 offset energy for the injection of both electrons and holes strongly limits charge injection into such systems, and therefore the excitation of Si NCs. Notwithstanding, matrix-embedded Si NC-based active layers show long-term operation, in contrast to the low-stable NPs, whose operation times are limited to some tens of hours due to NP migration towards the contacts when high electric fields are applied.[53] Finally, some groups have addressed the light extraction efficiency enhancement by taking advantage of a two-dimensional photonic crystal layer deposited as top electrode of Er^{3+}-doped Si NCs-based devices, which allows for precisely coupling, and thus enhancing, the Er^{3+} ions-related near-infrared emission.[54–56] This approach, compatible with Si technology, could be employed to enhance the visible-NIR emission from Si NCs.

In general, the published works so far have demonstrated that slight modifications on the NCs processing and distribution within the LED active layer, as well as the device design and the excitation conditions, result in different device efficiencies. In this frame, our design-improvement approach consists of depositing a controlled interlayer between substrate and Si NC superlattices, which favors minority carrier injection from the substrate and, consequently, electron-hole pair generation even in deep substrate inversion regime. Within this structure, the use of pulsed electrical excitation was found to increase the efficiency of the sequential carrier injection mechanism. In addition, the novelty of the design approach lays in the simplicity of the additional Si_3N_4 interlayer deposition step, which not only allows the application of planar technology, thus avoiding complex fabrication steps, but is also compatible with any existing device configuration strategy.

4. Conclusion

Light-emitting devices based on Si NCs have been fabricated via PECVD-deposited SRON/SiO_2 superlattices and a subsequent high-temperature annealing treatment. Our device structure consists in the addition of a 2-nm thick PECVD-deposited Si_3N_4 layer between the Si substrate and the SLs. The control sample structure contains both the nitride layer and a 10 nm SiO_2 carrier injection-blocking layer. The structural, optical, electrical and electro-optical properties of these LEDs have been studied. TEM analysis confirms the controlled deposition of the SLs as well as the additional nitride inversion layer and oxide blocking barrier. Electrical measurements revealed that the Si_3N_4 interlayer contains a high density of fixed positive charges that inverts the substrate. Due to continuous supply of electrons from the inversion layer around the electrode, the injection of electrons from the substrate into the SLs is significantly enhanced. This effect induces an enhancement of EL emission intensity, under pulsed excitation, with respect to the conventional Si NCs SLs-based device. In addition, EL yield is notably higher under pulsed electrical excitation, which is correlated to a more efficient sequential carrier injection. The best performance is achieved by devices containing the nitride interlayer under pulsed excitation, with a power efficiency of ~2.6×10^{-2}%, i.e., ~4 times higher than the conventional device structure. This efficiency increase confirms that our device design, i.e., the addition of a 2 nm Si_3N_4 interlayer, provides an easy approach to enhance the performance of Si NCs-based LEDs, by means of a fast technological process compatible with planar microelectronics. Overall, our hereby presented results pave the way for further improving the performance of light-emitting devices containing a Si NCs-based active layer.

5. Experimental Section

Material Preparation: The Si NCs/SiO_2 superlattices (SLs) were fabricated via the so-called superlattice approach.[57] Through this method, alternated Si-rich oxynitride (SRON, 4.5nm) and SiO_2 (1 nm) layers were deposited on top of *p*-type Si substrate ([B] ~ 10^{16} cm^{-3}, base resistivity of 1–20 Ω cm) by means of PECVD (deposition temperature of 375 °C). On top of such a structure, a 10 nm capping SiO_2 layer was also deposited by PECVD, followed by 10-nm amorphous Si and another 5 nm SiO_2 in order to protect the SLs from the subsequent high-temperature annealing treatment. After deposition, the samples were annealed at 1150 °C for 1 h under N_2 ambient in a quartz tube furnace, to induce the SRON Si excess precipitation and crystallization in the form of Si NCs. In addition, a H_2 passivation treatment was carried out at 450 °C for 1 h in pure H_2 gas, to get rid of undesired dangling bonds. After annealing, the 10-nm SiO_2 capping, amorphous Si and 5-nm SiO_2 protecting layers were selectively wet-chemically etched. More details on the Si NC SLs fabrication process are given in Ref. [28]. So far, the fabrication of the sample labeled as *NC* has been described. In sample *NC-SN*, an extra 2 nm Si_3N_4 layer was deposited between the Si substrate and the first SRON/SiO_2 bilayer via PECVD. In sample *NC-SN-SO*, additionally to the thin Si_3N_4 layer, a 10 nm SiO_2 layer was deposited on top of the SLs which was left unetched, to provide a blocking barrier for carriers from the top electrode.[34] In **Figure 2**, the details of the three different material structures can be observed.

Device Fabrication: The device structure was achieved by full-area evaporating the Si substrate rear side with Al, and depositing on top of the SLs a 100 nm ALD-ZnO (naturally *n*-type, resistivity < 0.01 Ω cm and ~75% transparency throughout the whole visible spectrum) using atomic layer deposition (ALD), at a deposition temperature of 200 °C.[50,58] The top ALD-ZnO electrode was patterned by conventional photolithography, achieving 500-µm-diameter circular-shaped contacts (i.e., total device area of ~2×10^{-3} cm^2). This way, an *N-I-P* design is achieved, being *N* the top *n*-type ALD-ZnO electrode, *I* (intrinsic) the Si NC SLs and *P* the *p*-type Si substrate. Further details on the device preparation can be found elsewhere.[19,34]

Material and Device Characterization: Direct observation of the sample structure was carried out via EFTEM and high-resolution TEM (HRTEM) using a JEOL 2010F instrument (field emission gun operating at 200 keV) equipped with a Gatan Image Filter (with a resolution of 0.8 eV), after preparing the samples by mechanical flat polishing and final low angle Ar^+ ion milling. In the case of EFTEM, the Si signal contrast was obtained by energetically filtering the electron energy-loss spectra around the Si plasmon energy (E_{Si} ~ 16.7 eV). PL spectra were acquired at room temperature by means of a LN_2-cooled CCD camera coupled to a high-spectral resolution single-grating monochromator, after exciting the material samples with the 325-nm

line of a He-Cd laser. Room temperature current-voltage [$I(V)$] and capacitance-voltage [$C(V)$, swept at a frequency of 300 kHz] measurements were performed in dark using high-resolution probes in a Microtech Summit 11000 probe station (equipped with a Faraday cage for electrical screening) coupled to an Agilent B1500 semiconductor device analyzer. When convenient for the study, electric field (E) was estimated by normalizing the applied voltage with the device thickness (i.e., Si NC superlattices + Si_3N_4 interlayer + SiO_2 injection barrier). After DC or pulsed electrical excitation, EL emission from the devices was collected using the 20× objective (NA = 0.4) of a Seiwa 888L microscope, and the spectra were acquired using a Princeton Instruments LN_2-cooled CCD coupled to a monochromator. All EL spectra were corrected by the system response. For quantitative EL PE measurements, the devices were placed at the entrance port of a 10-cm-diameter integrating sphere (absolutely calibrated using a 45-W tungsten-halogen lamp standard). Further details on the absolute emission efficiency measurements can be found in Ref. [42]. For time-resolved EL studies, the devices were excited with voltage pulses, and the resulting integrated EL was collected using a high-time resolution Agilent Infiniium DSO 8064A oscilloscope.

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References

[1] S. Furukawa, T. Miyasato, *Phys. Rev. B* **1988**, *38*, 5726.

[2] L. T. Canham, *Appl. Phys. Lett.* **1990**, *57*, 1046.

[3] F. Iacona, G. Franzò, C. Spinella, *J. Appl. Phys.* **2000**, *87*, 1295.

[4] F. Iacona, G. Franzo, *Opt. Mater.*. **2001**, *17*, 51.

[5] L. Khriachtchev, M. Räsänen, S. Novikov, L. Pavesi, *Appl. Phys. Lett.* **2004**, *85*, 1511.

[6] D. Kovalev, H. Heckler, G. Polisski, J. Diener, F. Koch, *Opt. Mater. (Amst).* **2001**, *17*,

35.

[7] K. Kůsová, P. Hapala, J. Valenta, P. Jelínek, O. Cibulka, L. Ondič, I. Pelant, *Adv. Mater. Interfaces* **2014**, *1*, 1300042.

[8] D. J. Dimaria, D. W. Dong, C. Falcony, T. N. Theis, J. R. Kirtley, J. C. Tsang, D. R. Young, F. L. Pesavento, *J. Appl. Phys.* **1983**, *54*, 5801.

[9] I. Balberg, E. Savir, J. Jedrzejewski, a. G. Nassiopoulou, S. Gardelis, *Phys. Rev. B - Condens. Matter Mater. Phys.* **2007**, *75*, 235329.

[10] I. Balberg, *J. Appl. Phys.* **2011**, *110*, 61301.

[11] G. Franzò, A. Irrera, E. C. Moreira, M. Miritello, D. Sanfilippo, G. Di Stefano, G. Fallica, F. Priolo, *Appl. Phys. A* **2002**, *74*, 1.

[12] A. Irrera, D. Pacifici, M. Miritello, G. Franzò, F. Priolo, F. Iacona, D. Sanfilippo, G. Di Stefano, P. G. Fallica, *Phys. E Low-dimensional Syst. Nanostructures* **2003**, *16*, 395.

[13] A. Fojtik, J. Valenta, T. H. Stuchlíková, J. Stuchlík, I. Pelant, J. Kočka, *Thin Solid Films* **2006**, *515*, 775.

[14] D. Jurbergs, E. Rogojina, L. Mangolini, U. Kortshagen, *Appl. Phys. Lett.* **2006**, *88*, 2004.

[15] J. Valenta, M. Greben, S. Gutsch, D. Hiller, M. Zacharias, *Appl. Phys. Lett.* **2014**, *105*, 243107.

[16] G. Conibeer, M. Green, R. Corkish, Y. Cho, E.-C. Cho, C.-W. Jiang, T. Fangsuwannarak, E. Pink, Y. Huang, T. Puzzer, T. Trupke, B. Richards, A. Shalav, K. Lin, *Thin Solid Films* **2006**, *511–512*, 654.

[17] A. Marconi, A. Anopchenko, M. Wang, G. Pucker, P. Bellutti, A. Marconi, A. Anopchenko, M. Wang, G. Pucker, P. Bellutti, L. Pavesi, *Appl. Phys. Lett.* **2013**, *94*, 221110.

[18] A. Anopchenko, A. Marconi, E. Moser, S. Prezioso, M. Wang, L. Pavesi, G. Pucker, P. Bellutti, *J. Appl. Phys.* **2009**, *106*, 33104.

[19] J. López-Vidrier, Y. Berencén, S. Hernández, O. Blázquez, S. Gutsch, J. Laube, D. Hiller, P. Löper, M. Schnabel, S. Janz, M. Zacharias, B. Garrido, *J. Appl. Phys.* **2013**, *114*, 163701.

[20] J. Lopez-Vidrier, Y. Berencén, S. Hernández, B. Mundet, S. Gutsch, J. Laube, D. Hiller, P. Löper, M. Schnabel, S. Janz, M. Zacharias, B. Garrido, *Nanotechnology* **2015**, *26*, 185704.

[21] R. J. Walters, G. I. Bourianoff, H. A. Atwater, *Nat. Mater.* **2005**, *4*, 143.

[22] R. J. Walters, J. Carreras, T. Feng, L. D. Bell, H. A. Atwater, *IEEE J. Sel. Top. Quantum Electron.* **2006**, *12*, 1647.

[23] M. Perálvarez, C. García, M. López, B. Garrido, J. Barreto, C. Domínguez, J. A Rodríguez, *Appl. Phys. Lett.* **2006**, *89*, 51112.

[24] M. Perálvarez, J. Carreras, J. Barreto, A. Morales, C. Domínguez, B. Garrido, *Appl. Phys. Lett.* **2008**, *92*, 241104.

[25] J. Carreras, J. Arbiol, B. Garrido, C. Bonafos, J. Montserrat, *Appl. Phys. Lett.* **2008**, *92*, 091103.

[26] T. Creazzo, B. Redding, E. Marchena, J. Murakowski, D. W. Prather, *Opt. Express* **2010**, *18*, 10924.

[27] Y. Berencén, J. M. Ramírez, O. Jambois, C. Domínguez, J. A. Rodríguez, B. Garrido, *J. Appl. Phys.* **2012**, *112*, 33114.

[28] A. M. Hartel, D. Hiller, S. Gutsch, P. Löper, S. Estradé, F. Peiró, B. Garrido, M. Zacharias, *Thin Solid Films* **2011**, *520*, 121.

[29] J. López-Vidrier, S. Hernández, a. M. Hartel, D. Hiller, S. Gutsch, P. Löper, L. López-Conesa, S. Estradé, F. Peiró, M. Zacharias, B. Garrido, *Energy Procedia* **2011**, *10*, 43.

[30] A. Eljarrat, L. López-Conesa, J. López-Vidrier, S. Hernández, B. Garrido, C. Magén, F. Peiró, S. Estradé, *Nanoscale* **2014**, *6*, 14971.

[31] J. López-Vidrier, S. Hernández, D. Hiller, S. Gutsch, L. López-Conesa, S. Estradé, F.

Peiró, M. Zacharias, B. Garrido, *J. Appl. Phys.* **2014**, *116*, 133505.

[32] A. M. Hartel, S. Gutsch, D. Hiller, M. Zacharias, C. Kübel, N. Zakharov, P. Werner, *Appl. Phys. Lett.* **2012**, *101*, 193103.

[33] A. Zelenina, S. A. Dyakov, D. Hiller, S. Gutsch, V. Trouillet, M. Bruns, S. Mirabella, P. Löper, L. López-Conesa, J. López-Vidrier, S. Estradé, F. Peiró, B. Garrido, J. Bläsing, A. Krost, D. M. Zhigunov, M. Zacharias, *J. Appl. Phys.* **2013**, *114*, 184311.

[34] S. Gutsch, J. Laube, A. M. Hartel, D. Hiller, N. Zakharov, P. Werner, M. Zacharias, *J. Appl. Phys.* **2013**, *113*, 133703.

[35] M. A. Lampert, R. B. Schilling, *Semicond. Semimetals* **1970**, *6*, 1.

[36] S. Tondini, G. Pucker, L. Pavesi, *J. Appl. Phys.* **2016**, *120*, 093108.

[37] J. Valenta, N. Lalic, J. Linnros, *Opt. Mater.* **2001**, *17*, 45.

[38] S. Tondini, G. Pucker, L. Pavesi, *J. Phys. D. Appl. Phys.* **2015**, *48*, 455103.

[39] J. Valenta, M. Greben, Z. Remeš, S. Gutsch, D. Hiller, M. Zacharias, *Appl. Phys. Lett.* **2016**, *108*, 023102.

[40] M. Kulakci, U. Serincan, R. Turan, T. G. Finstad, *Nanotechnology* **2008**, *19*, 455403.

[41] J. López-Vidrier, S. Gutsch, O. Blázquez, D. Hiller, J. Laube, R. Kaur, S. Hernández, B. Garrido, M. Zacharias, *Appl. Phys. Lett.* **2017**, *110*, 203104.

[42] J. Valenta, *Nanosci. Methods* **2014**, *3*, 11.

[43] N. Lalic, J. Linnros, *J. Appl. Phys.* **1996**, *80*, 5971.

[44] J. Linnros, N. Lalic, A. Galeckas, V. Grivickas, *J. Appl. Phys.* **1999**, *86*, 6128.

[45] M. Dovrat, Y. Goshen, J. Jedrzejewski, I. Balberg, a. Sa'ar, *Phys. Rev. B - Condens. Matter Mater. Phys.* **2004**, *69*, 155311.

[46] A. J. Morfa, B. C. Gibson, M. Karg, T. J. Karle, A. D. Greentree, P. Mulvaney, S. Tomljenovic-Hanic, *Nano Lett.* **2012**, *12*, 949.

[47] J. F. Verwey, E. A. Amerasekera, J. Bisschop, *Reports Prog. Phys.* **1990**, *53*, 1297.

[48] M. Perálvarez, J. Barreto, J. Carreras, A. Morales, D. Navarro-Urrios, Y. Lebour, C.

Domínguez, B. Garrido, *Nanotechnology* **2009**, *20*, 405201.

[49] H. Beh, D. Hiller, J. Laube, S. Gutsch, M. Zacharias, *J. Vac. Sci. Technol. A Vacuum, Surfaces, Film.* **2017**, *35*, 01B127.

[50] J. Laube, D. Nübling, H. Beh, S. Gutsch, D. Hiller, M. Zacharias, *Thin Solid Films* **2016**, *603*, 377.

[51] K. Y. Cheng, R. Anthony, U. R. Kortshagen, R. J. Holmes, *Nano Lett.* **2011**, *11*, 1952.

[52] F. Maier-Flaig, J. Rinck, M. Stephan, T. Bocksrocker, M. Bruns, C. Kübel, A. K. Powell, G. a. Ozin, U. Lemmer, *Nano Lett.* **2013**, *13*, 475.

[53] F. Maier-Flaig, C. Kübel, J. Rinck, T. Bocksrocker, T. Scherer, R. Prang, A. K. Powell, G. A. Ozin, U. Lemmer, *Nano Lett.* **2013**, *13*, 3539.

[54] M. Galli, A. Politi, M. Belotti, D. Gerace, M. Liscidini, M. Patrini, L. C. Andreani, M. Miritello, A. Irrera, F. Priolo, Y. Chen, *Appl. Phys. Lett.* **2006**, *88*, 251114.

[55] L. Ondič, M. Varga, K. Hruška, A. Kromka, K. Herynková, B. Hönerlage, I. Pelant, *Appl. Phys. Lett.* **2013**, *102*, 251111.

[56] R. Lo Savio, M. Galli, M. Liscidini, L. C. Andreani, G. Franzò, F. Iacona, M. Miritello, A. Irrera, D. Sanfilippo, F. Priolo, F. Iacona, M. Miritello, *Appl. Phys. Lett.* **2014**, *104*, 121107.

[57] M. Zacharias, J. Heitmann, R. Scholz, U. Kahler, M. Schmidt, J. Bläsing, *Appl. Phys. Lett.* **2002**, *80*, 661.

[58] H. Beh, D. Hiller, M. Bruns, A. Welle, H. W. Becker, B. Berghoff, C. Sürgers, R. Merz, M. Zacharias, *J. Appl. Phys.* **2017**, *122*, 025306.