# Low-noise pixel detectors based on gated Geiger mode avalanche photodiodes

E. Vilella, A. Comerma, O. Alonso and A. Diéguez

The gated operation is proposed as an effective method to reduce the noise in pixel detectors based on Geiger mode avalanche photodiodes. A prototype with the sensor and the front-end electronics monolithically integrated has been fabricated with a conventional HV-CMOS process. Experimental results demonstrate the increase of the dynamic range of the sensor by applying this technique.

*Introduction:* Avalanche photodiodes reverse biased above the breakdown voltage ($V_{BD}$) in the so-called Geiger mode (GAPDs) can be used to detect single charge carriers thanks to the self-sustaining avalanche multiplication process, provided that proper quenching and readout electronics are employed [1]. In particular, the high intrinsic sensitivity of GAPDs together with the feasibility of on-chip integration of the sensor and the front-end electronics enabled by CMOS technologies [2] can be of benefit in various fields, such as 3D imaging for bio-applications, time-of-flight (TOF) ranging, astronomical observations and high energy physics (HEP) experiments [3]. However, the high intrinsic gain also generates false avalanches that cannot be distinguished from real events and increases the intrinsic sensor noise. Spurious avalanches caused by thermal or tunnel carriers are called dark counts. The dark count rate (DCR) depends on the technology, the sensitive area, the reverse bias overvoltage ($V_{OV}$) and the temperature. Moreover, correlated pulses due to the random release of carriers that were trapped during a previous avalanche are known as afterpulses. The afterpulsing probability is a function of the trap density, the number of carriers involved in an avalanche and the lifetime of these carriers.

The efforts reported in the literature related to the reduction of the noise in GAPD detectors consider dedicated technologies [4] and quenching circuits that delay the recharge of the device [5] or minimise either the charge flow [6] or the duration of the avalanche process [7]. Whereas the former requires high-cost technologies, the last three consider only the reduction of afterpulses. Apart from that, in those applications in which the arrival time of charge carriers is known it is also possible to use the gated mode operation to improve the performance of the detector. Although this technique has already been used to reduce dark counts and afterpulses in InGaAs/InP detectors [8], to the best of our knowledge it is the first time that the gated acquisition for decreasing the noise in a GAPD pixel detector monolithically integrated is reported.

*Experiment:* The sensor integrated with the proposed front-end circuit was prototyped in the standard HV-AMS 0.35 µm CMOS technology (h35b4). The pixel detector characterised in this work corresponds to AMS R2 CX 20 × 100 2G, where the nomenclature stands for technology, run, chip, size of the sensor (in µm) and readout circuit. Dark counts were obtained by making a statistical analysis of the number of pulses generated by the sensor in 100 000 repetitions ($n_{rep}$) of the gated cycle ($t_{cycle}$) for different reverse bias overvoltages (0.5, 1.0 and 1.5 V, provided that $V_{BD}$ is set at 18.9 V) and different periods of observation (from 10 to 1280 ns). These measurements were performed using an Agilent E3631A voltage source to power the pixels and an FPGA to generate the fast logic control signals and count the pulses. The dynamic range of the pixel detectors to light was also measured using a red LED (650 nm) placed over the sensor. The whole system was placed inside a metallic black box to protect the circuit from uncontrolled light sources. The light emitter was powered using an HP 3245A universal source and the current flowing through it was measured by means of an HP 3458A multimeter.

*Proposed circuit:* A schematic diagram of the proposed pixel detector based on a gated GAPD (GGAPD) with passive quenching and active recharge (PQAR) is shown in Fig. 1. The gated mode operation is controlled through three external signals implemented by means of MOS transistors. The gated 'on' time or period of observation ($t_{obs}$) starts when an nMOS transistor (RST) connected between the sensing node ($V_S$) and ground clears $V_S$ by quickly restoring the reverse bias voltage of the sensor (≤3 ns), thus enabling the pixel for the detection of the next GAPD firing. At the same time, an nMOS pass gate (CLK1) is enabled to store the final value of $V_S$ during the whole

gated 'off' period. The time in which the CLK1 transistor is active determines the duration of $t_{obs}$. However, since the sensor can be triggered during the reset phase, the rising edges of the RST and CLK1 signals need to be synchronised in order to avoid missing counts and obtain a high detection linearity. These missing counts, known as extended pulses, are present in all circuits employing an active reset. Finally, a pMOS transistor (INH) connected between $V_{DD}$ and $V_S$ lowers the reverse bias voltage of the sensor below $V_{BD}$ after $t_{obs}$, thus inhibiting charge carrier detection and reducing power consumption during the 'off' period. The INH transistor is disabled before a new $t_{obs}$ starts. As a consequence of this configuration, $V_{OV}$ is limited to $V_{DD}$. The sequence of waveforms to control the GGAPD is also depicted in Fig. 1.
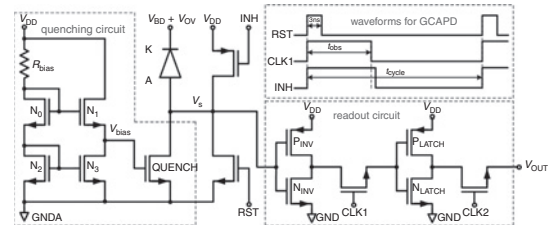


**Fig. 1** *Schematic diagram of proposed pixel detector together with waveforms for gated acquisition*

During $t_{obs}$, the GGAPD is biased between a positive high voltage value set by $V_{BD} + V_{OV}$ and a negative $V_S$ connected to the quenching and readout circuits. Instead of the typical resistor connected in series with the sensor, the quenching circuit has been implemented by means of an active load based on an nMOS transistor (QUENCH) with proper ($W/L$) ratio and bias voltage ($V_{bias}$) in order to save area. Thanks to the bias circuit, the resistance of the QUENCH transistor has been adjusted to a high value of 360 kΩ to provide a prompt passive quenching of the avalanche and minimise the afterpulsing probability, but it could be further increased if necessary.

When an avalanche is triggered, the voltage of $V_S$ rapidly swings from ground to $V_{OV}$ until the quenching is performed. To achieve low dark count rates and high fill factors, low reverse bias overvoltages and minimum area readout circuits are desired, respectively. Consequently, readout circuits capable of low voltage detection implemented in a reduced area are required. However, the threshold voltage of the MOS transistors of the standard 0.35 µm CMOS technology ($V_{Thn} = 0.5$ V) represents a constraint to this specification. To overcome this drawback, a strategy that makes use of a two grounds scheme (2G) has been used in this work. The ground of the sensor (GNDA) is raised with regard to the ground of the electronics (GND), so that the avalanche voltage ($V_{OV}$) is easily detected by a simple CMOS inverter, the threshold voltage of which is set at $V_{DD}/2$. In addition, a dynamic latch (controlled by CLK1) has been added to store the final value of $V_S$ at the end of $t_{obs}$. Finally, a pass gate (CLK2) allows the reading of the pixel out during the 'off' period.
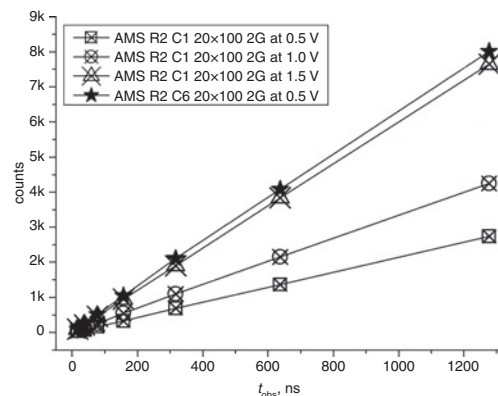


**Fig. 2** *Dark counts of proposed pixel detector of different chips for several $V_{OV}$ against $t_{obs}$*

*Measured results and discussion:* The data extracted from the statistical analysis is shown in Fig. 2, where it has been represented as the number of dark counts as a function of the duration of $t_{obs}$. In these

measurements afterpulses are avoided leaving sufficiently long 'off' periods of 300 ns [7]. 'Off' times of 300 ns are enough for these pixels. First, the dark counts of AMS R2 C1 20 × 100 2G have been plotted for different $V_{OV}$ (0.5, 1.0 and 1.5 V). As expected, the number of counts increases with $V_{OV}$ and also with $t_{obs}$, which confirms that GGAPDs are efficient for reducing the number of observed dark counts. Secondly, the dark counts of AMS R2 C6 20 × 100 2G at 0.5 V are also shown. Large variations between pixels of different chips indicate that the measurements are not affected by the readout circuit and that the dark counts are randomly generated.

The dynamic range (DR) of the proposed pixel to light is shown in Fig. 3. The measurement has been performed with a fixed $V_{OV}$ of 0.5 V for three different $t_{obs}$ (20, 200, 1280 ns). In all the cases, the total time of the measurement is given by $n_{rep} t_{obs}$, where $n_{rep}$ is 100 000 repetitions. As expected, the experimental results show a proportional increase of the number of pulses generated in the sensor with the increase of light, until saturation. This results in a lower intrinsinc noise floor as $t_{obs}$ is reduced. As a consequence, the lower level of light detected is lower as $t_{obs}$ is decreased (dynamic range increased), which also results in a better definition of the high intensity region. As seen in Fig. 3, while a dynamic range of 9 bits is obtained for a $t_{obs}$ of 1280 ns, it can be extended up to 14 bits when $t_{obs}$ is reduced down to 20 ns. Therefore, it can be concluded that GGAPDs with shorter $t_{obs}$ enable an extension of the dynamic range of the sensor and thus an increase of the resolution of the pixel.
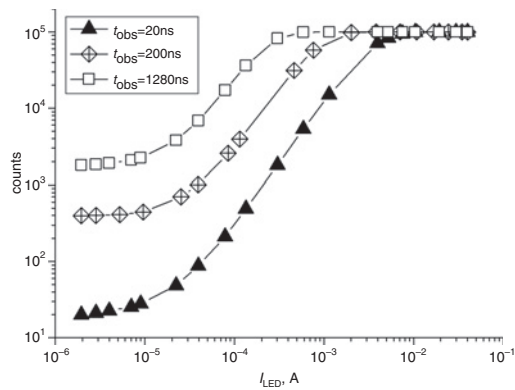


**Fig. 3** *Dynamic range of AMS R2 C1 20 × 100 2G at 0.5 V for different $t_{obs}$*

*Conclusions:* A novel pixel detector to operate GAPDs in a gated acquisition mode is presented. The proposed mode of operation, together with suitable readout electronics that allow low reverse bias overvoltages, has been proved effective to reduce the noise in a pixel. Moreover, gating with lower periods of observation allows a considerable increase in the dynamic range of the sensor.

E. Vilella, O. Alonso and A. Diéguez (*Department of Electronics, University of Barcelona, Martí i Franquès 1, 08020-Barcelona, Spain*)

E-mail: evilella@el.ub.es

A. Comerma (*Department of Structure and Constituents of Matter, University of Barcelona, Martí i Franquès 1, 08020-Barcelona, Spain*)

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