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Low Dark Count Geiger Mode Avalanche Photodiodes Fabricated in Conventional CMOS Technologies

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Avalanche photodiodes operated in the Geiger mode present very high intrinsic gain and fast time response, which make the sensor an ideal option for those applications in which detectors with high sensitivity and velocity are required. Moreover they are compatible with conventional CMOS technologies, allowing sensor and front-end electronics integration within the pixel cell. Despite these excellent qualities, the photodiode suffers from high intrinsic noise, which degrades the performance of the detector and increases the memory area to store the total amount of information generated. In this work, a new front-end circuit that allows low reverse bias overvoltage sensor operation to reduce the noise in Geiger mode avalanche photodiode pixel detectors is presented. The proposed front-end circuit also enables to operate the sensor in the gated acquisition mode to further reduce the noise. Experimental characterization of the fabricated pixel with the conventional HV-AMS 0.35 μm technology is also presented in this article.

Keywords: Geiger Mode Avalanche Photodiodes, Dark Count, Gated Acquisition Mode, Low Reverse Bias Overvoltage, Pixel, Track-and-Latch Comparator.

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1. INTRODUCTION

The virtually infinite internal gain and accurate time response of avalanche photodiodes reverse biased above the breakdown voltage (V_{BD}) in the so-called Geiger mode (GAPDs),[1] together with the capabilities offered by CMOS technologies,[2] can be of benefit in many fields. These fields range from low-level light detection, like biomedical imaging or fluorescence measurements, to high speed detectors used in time of flight (TOF) applications or in high energy physics (HEP) experiments. However, the high intrinsic gain of GAPDs also generates false avalanches that cannot be distinguished from real events and reduce the performance of the detector. Spurious avalanches generated by thermal or tunnel carriers are called dark counts. The dark count rate (DCR), which is defined as the number of false counts per second, depends on the technology, the sensitive area, the reverse bias overvoltage (V_{OV}) and the temperature. Moreover, released carriers that were trapped during a previous avalanche are known as afterpulses. The afterpulsing probability is a function of the trap density, the number of carriers involved in an avalanche and the lifetime of these carriers.

In order to overcome the performance limitation introduced by the noise, it is necessary to explore new solutions such as the utilization of dedicated or older technologies with lower doping profiles, the development of GAPD pixels vertically integrated[3] or the introduction of cooling systems. In particular, this work is focused on the development of a new front-end circuit with the HV-AMS 0.35 μm conventional CMOS technology that allows low noise operation thanks to the introduction of two concepts at the readout level. In the first place, given that the dark count rate strongly depends on the reverse bias overvoltage of the sensor, the reduction of V_{OV} to few mV should enable a dramatic decrease of the dark counts. In the second place, as the dark count rate is a random phenomenon, if the active period of the sensor is reduced while synchronized with the expected signal arrival in a gated acquisition mode,[4] the number of dark counts should be further reduced without losing information. In addition, it should also be possible to eliminate the presence of afterpulses by leaving long enough non-active periods between one beam and the next one.

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2. EXPERIMENTAL METHODS

2.1. Sensor Technology

A comparison between two standard CMOS technologies, which are the HV-AMS 0.35 μm and the STM 0.13 μm, for the fabrication of GAPDs has already been presented.[5] Although a further analysis with temperature and on irradiated sensors has to be performed to have more concluding results, the lower dark count rate of the HV-AMS 0.35 μm technology associated to its lower trap concentration has made us to continue working with this technology in order to develop low noise detectors. The prototype presented in this work corresponds to our second run with the HV-AMS 0.35 μm technology (h35b4) to study and characterize avalanche photodiodes, where the sensor has been monolithically integrated with the front-end electronics on a single CMOS die. The sensor size is 20 μm $\times$ 100 μm. The avalanche diode is implemented by means of a p^+/n-well junction with a p-well guard ring to prevent premature edge breakdown. The details of the sensor structure have been previously described.[5]

2.2. Front-End Circuit

The front-end circuit is composed of quenching and readout electronics, which are discussed next. A schematic of the proposed pixel detector is shown in Figure 1.

2.2.1. Quenching and Recharge Circuits

The quenching electronics, which lowers the bias of the sensor below its V_{BD} to stop the avalanche in order to avoid burning the device, is usually implemented by passive or active components, although mixed solutions are also possible.[6] In the proposed pixel, instead of the typical resistor connected in series with the sensor, the quenching electronics has been implemented by means of an active load based on an nMOS transistor.[7] Thereby, the total occupied area is reduced and the fill factor is increased.

2.2.2. Readout Circuit

When an avalanche is triggered, the voltage of the sensing node (V_S) rapidly swings from ground to V_{OV} until the quenching is done. Avalanche detection is performed by the readout electronics, which is normally implemented by means of a simple CMOS inverter. However, as a consequence of the threshold voltage of the MOS transistors ($V_{Thn} = 0.5$ V in this process), an inverter does not allow low reverse bias voltage operation. To overcome this drawback, in this work we have implemented a low noise readout circuit based on a track-and-latch comparator.[8] In this design, the threshold voltage of the MOS transistors is not a drawback since the input differential pair is implemented with pMOS transistors.

The operation of the track-and-latch comparator is as follows. During the so-called track phase or period of observation (t_{obs}) (CLK1 = '1'), transistors P_1 and P_2 sample the two input nodes, which correspond to the avalanche voltage (V_S) and a reference voltage (V_{REF}). As a result, the channel current of these transistors is modulated. However, nodes V_{out+} and V_{out-} are shorted to ground and the injected charge remains accumulated at the drain nodes of P_1 and P_2. In contrast, during the latch phase (CLK1 = '0') transistors N_1 and N_2 are turned off, the comparison is rapidly performed and a decision is taken in picoseconds. Thus, if V_S is higher than V_{REF} (i.e., there has been an avalanche), the accumulated charge at the drain node of P_1 at the end of the track phase is higher than the charge at drain node of P_2. In this situation, a logic '1' will be stored by node V_{out+} whereas V_{out-} will be set at a logic '0'. The opposite values are generated when there has been no avalanche.

Readout circuits that allow low reverse bias overvoltage operation to reduce the dark count rate have already been

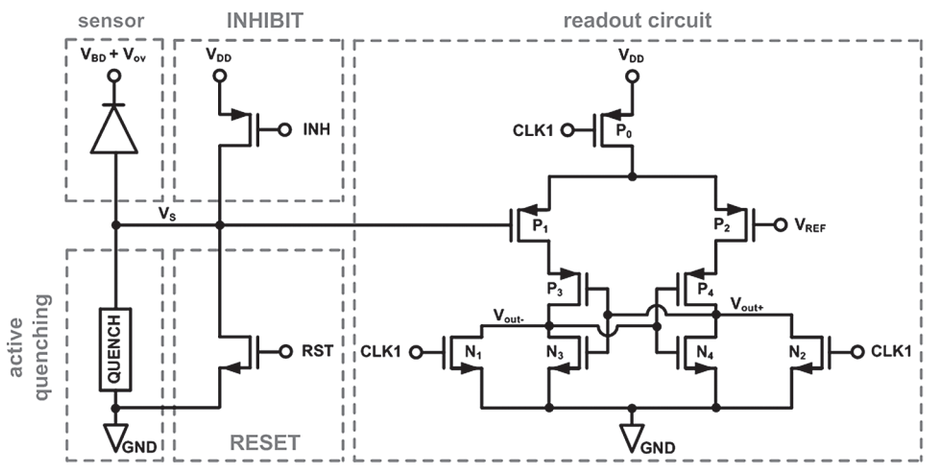

Fig. 1. Generic schematic diagram of the proposed pixel detector, with the sensor, the active quenching, the logic control switches and the readout circuit based on a track-and-latch comparator.

reported.[9] The circuit proposed in the present article has the advantages of using only one ground node, an integrated latch with the comparator and a higher (15 times) readout speed. To further reduce the noise, the sensor is active only during short periods of time which are synchronized with the expected signal arrival. In this mode of operation, known as gated acquisition,[9] the reverse bias voltage of the sensor is kept above V_{BD} at the desired reverse bias overvoltage for the active periods, and reduced below V_{BD} during the non-active times. In the pixel presented in this work, it is controlled by three external signals (RST, CLK1 and INH), which recharge the sensor, enable the readout circuit to sample the sensing node during t_{obs}, latch the last value of V_S and finally disable sensor operation during the non-active periods.

2.3. Test Set-Up

Together with the pixel detector, in the same run we also included some test photodiodes with the same sensitive area for the $I(V)$ characterization in order to obtain the operation point of the sensor. For this purpose, we used a four wire method implemented by means of a Keithley 2611A source connected to the terminals of the sensor. The test was done inside a metallic box that provides electromagnetical and luminous protection to the circuit. The DCR of the proposed pixel detector was obtained by making a statistical analysis of the number of pulses generated by the sensor in 100000 repetitions (n_{rep}) of the gated cycle (comprised of the active and non-active periods of the sensor). Different reverse bias overvoltages (0.5 V, 1.0 V and 1.5 V) were used to prove that the DCR is reduced with lower V_{OV}. Also, different active periods (from 50 ns to 250 ns) were set to analyze the efficiency of the gated acquisition. For these measurements, we used an Agilent E3631A voltage source to power the pixel and an FPGA to generate the fast logic control signals as well as to make the reaout off-chip.

3. RESULTS AND DISCUSSION

The data extracted from the statistical analysis performed at room temperature is shown in Figure 2, where the dark count rate has been represented in function of the duration of the period of observation for different values of the reverse bias overvoltage (0.5 V, 1.0 V and 1.5 V, provided that the breakdown voltage is set at 18.94 V). In these measurements afterpulses were avoided by leaving sufficiently long non-active periods of 300 ns, which are enough for these pixels.[10] First, we have detected that the DCR decreases linearly with V_{OV}, as expected. This also confirms that the track-and-latch comparator is capable of working with low V_{OV}. Second, we have observed that the DCR is constant despite the value of t_{obs}, which implies that the number of dark counts is reduced for shorter t_{obs}

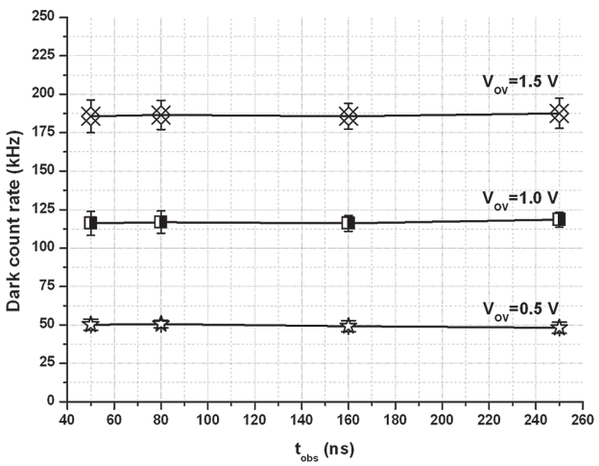

Fig. 2. Dark count rate in function of the period of observation for the proposed pixel at different reverse bias overvoltages.

as it can be deduced from $dark\ counts = DCR \cdot t_{obs}$. Given that the dark count rate is a random phenomenon, if the sensor is active only during short discrete intervals in the nanosecond range, the probability to detect a dark count is dramatically reduced. In addition, the gated acquisitioin also allows to synchronize the period of observation of the sensor with the expected signal arrival. Short gated 'on' periods of a few nanoseconds are enough for the applications of the state-of-the-art. As a consequence, the efficiency of the sensor is improved without any loss of information. We can conclude that the proposed readout circuit together with the gated acquisition constitute an effective method to reduce the noise in a GAPD pixel.

4. CONCLUSION

A new low-noise GAPD pixel detector fabricated in a conventional HV-AMS 0.35 μm technology has been studied and characterized. The GAPD pixel detector includes a readout circuit based on a track-and-latch comparator that can cope with low reverse bias overvoltages to reduce the dark count noise. In addition, the sensor can be operated in the gated acquisition, thereby enabled for detection only for short and well defined time intervals that are coincident with the expected signal arrival. As a consequence of the inhibition of the sensor during the gated 'off' times, afterpulses are eliminated. Short gated 'on' periods also allow a further reduction of the dark count noise. Compared with other readout circuits of the literature, the presented prototype offers the advantages of a reduced complexity in biasing, an integrated latch with the comparator and a higher (15 times) readout speed.

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