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Avoiding sensor blindness in Geiger mode avalanche photodiode arrays fabricated in a conventional CMOS process

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ABSTRACT: The need to move forward in the knowledge of the subatomic world has stimulated the development of new particle colliders. However, the objectives of the next generation of colliders sets unprecedented challenges to the detector performance. The purpose of this contribution is to present a bidimensional array based on avalanche photodiodes operated in the Geiger mode to track high energy particles in future linear colliders. The bidimensional array can function in a gated mode to reduce the probability to detect noise counts interfering with real events. Low reverse overvoltages are used to lessen the dark count rate. Experimental results demonstrate that the prototype fabricated with a standard HV-CMOS process presents an increased efficiency and avoids sensor blindness by applying the proposed techniques.

KEYWORDS: Front-end electronics for detector readout; VLSI circuits; Analogue electronic circuits

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Contents

1	Introduction	1
2	Geiger mode avalanche photodiodes	2
3	Detector design and operation	3
4	Results and discussion	5
5	Conclusion	7

1 Introduction

Each generation of High Energy Physics (HEP) experiments is related to its own technology of accelerators and detectors. Currently, the Large Hadron Collider (LHC) is run with the main expectancy to test the last missing piece of the Standard Model (SM) of particle physics, the Higgs boson. At LHC two circulating beams of protons or heavy ions are made to collide each $0.025\mu\text{s}$ with a beam energy of 7 TeV. However, steps are already being taken towards a new generation of particle colliders in order to explore the possibilities of physics beyond the SM. Although there is now a worldwide consensus for a e^+e^- high precision linear collider, some of the characteristics have not been decided yet. In fact, two solid projects with different bunch crossing (BX) rates and beam energies, amongst other differences, are ongoing. On the one hand, the International Linear Collider (ILC) proposes 5 trains per second, with 2820 BXs per train and an interbunch spacing of 337ns (intertrain period of 200ms). According to this project, the beam energy can be up to 1 TeV. On the other hand, the Compact Linear Collider (CLIC) suggests 50 trains per second, with 312 BXs 0.5ns apart (intertrain period of 20ms) and a beam energy up to 3TeV.

Appropriate detector systems capable of precisely measuring the direction of particle tracks are needed in order to fully exploit the research potential of any particle accelerator. Nevertheless, future e^+e^- linear colliders put challenging requirements on detector systems since they will have to supply unprecedented position resolution at high incoming rates. At present time, there is no mature technology that can fulfill these specifications [1, 2] and new detector systems are being developed in parallel with the accelerator. Solid-state sensor technologies concentrating most of the research are based on CMOS monolithic pixel sensors, which are Charge Coupled Devices (CCDs) [3], Monolithic Active Pixel Sensors (MAPS) [4] and DEPLETED Field Effect Transistors (DEPFETs) [5]. Alternative approaches are Silicon-On-Insulator (SOI) [6] devices and Geiger mode Avalanche PhotoDiodes (GAPDs) [7]. Although all of them could do the job, none of the presented candidates meets all the requirements imposed by the collider and several research groups are already working towards their improvement. More recently, CMOS sensors exploiting vertical integration technology are also under study [8]. This alternative may have the highest potential, but it will need more time to reach maturity.

Detector systems for efficient particle detection in future linear colliders must cope also with the occupancy induced by the background hits in the beam pipe region. If the detector, composed of several sensors and their corresponding readout electronics, is not fast enough to time-stamp the individual BX, then the background of several BXs will have to be accumulated. However, given the high incoming event rate, single BX readout is preferred. CCDs, MAPS and DEPFETs, for instance, take several microseconds to read the whole detector. In contrast, due to their virtually infinite intrinsic gain (10^5 - 10^6), GAPDs generate an output signal within a few hundred picoseconds after the event. Provided that fast enough readout electronics are used, GAPD detectors can be read out in nanoseconds, which makes them a very interesting option. Currently, they are the only candidates that allow single BX detection.

Owing to their high intrinsic gain, GAPDs can generate noise counts which cannot be separated from real events. In addition, noise counts can also cause sensor blindness, situation in which no detection is possible. In this article, we present a GAPD detector with the sensor and the front-end electronics monolithically integrated with the standard HV-AMS $0.35\mu\text{m}$ CMOS technology (h35b4) that makes use of two techniques to reduce the noise. On the one hand, the sensor can function with low biases to reduce the intrinsic noise. On the other hand, the sensor can be operated in a gated mode that can be synchronized with the BX to reduce the probability to detect noise counts without missing any real hits. No cooling methods or digital processing have been used to diminish noise figures.

2 Geiger mode avalanche photodiodes

A GAPD is based on a p-n junction reverse biased above its breakdown voltage (V_{BD}). Given the high electric field that is generated within the junction area, ionizing radiation that is absorbed by the material may give rise to the prompt generation of a detectable macroscopic current pulse. This current continues to flow until it is stopped by the quenching electronics, which lowers the reverse bias voltage (V_{OV}) down to or below V_{BD} . In the last place, the bias of the sensor has to be restored so that upcoming radiation can be detected.

Due to the high intrinsic gain of the sensor, thermal and tunneling generated carriers within the p-n junction can also trigger avalanche pulses that are indistinguishable from real events. The frequency of generation of these spurious pulses, known as dark count rate (DCR) and usually expressed in Hz, depends on the technology, the sensor area, the reverse bias overvoltage over V_{BD} and the temperature. Moreover, charge carriers that were trapped by crystal defects during a previous avalanche flow also generate false pulses when they are released at a certain time delay and re-trigger the GAPD. The afterpulsing probability is a function of the trap density, the number of carriers generated during an avalanche and the release time of these carriers. Both dark counts and afterpulses degrade the performance of the sensor, leading to erroneous results and increasing the amount of data that has to be stored for the subsequent processing. Apart from that, given the extreme dependence of the DCR on the cleanliness of the fabrication process, an excessively irregular DCR distribution may appear amongst the pixels of GAPD detectors [9]. Point defects in the crystal lattice, such as clusters of impurities or dislocations, may also lead to defective pixels with noise levels well above the acceptable threshold. These pixels, called dead pixels or hot pixels, represent a serious problem as they reduce the sensitive area.

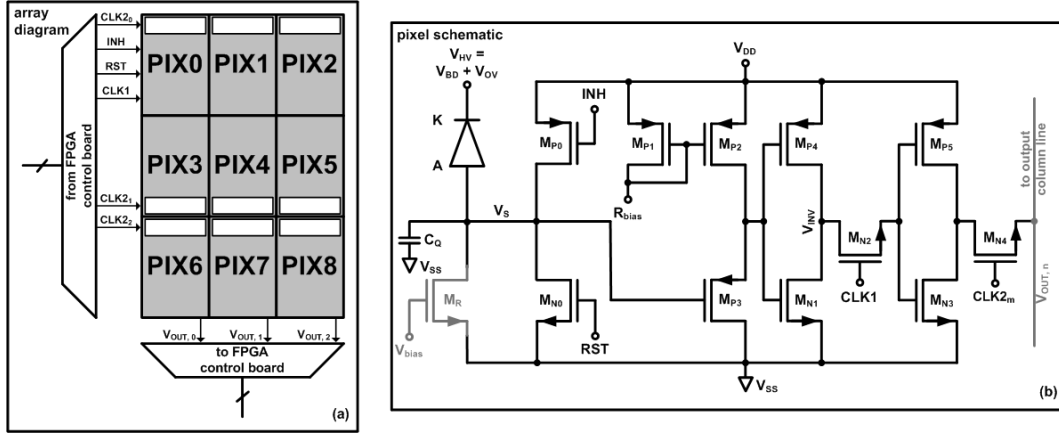


Figure 1. Block diagram of the 3×3 GAPD array (a) and schematic of the proposed digital pixel (b).

Solutions commonly adopted to reduce the noise in GAPD detectors regard dedicated technologies with lower doping profiles [10], cooling methods either with Peltier elements [11] or air cooling [12], and advanced front-end circuits that minimize the avalanche charge flow [13]. Dead pixels are simply switched off by means of digital processing [14]. However, none of the presented techniques is completely satisfactory given the high costs of fabrication of dedicated technologies, the reduced applicability of cooling methods, the reduced fill-factor of advanced front-end circuits or the severe loss of sensitive area induced by switching off dead pixels. Apart from that, in those applications where the signal arrival time is known, as happens in HEP experiments, the sensor can be operated using gated data acquisition. In contrast with the free-running mode of operation, where the sensor is always reverse biased above V_{BD} at a fixed voltage, in the gated acquisition the reverse bias voltage swings from over to under V_{BD} to periodically enable and disable the photodiode. The sensor is kept active only for short periods of time that can be synchronized with the BX. Consequently, the probability to detect dark counts interfering with radiation-triggered counts (known as dark count probability or DCP) is linearly reduced with the width of the active period of the sensor without missing any real events. In addition, long enough non-active periods, longer than the lifetime of the trapping levels, allow to completely eliminate the afterpulsing probability [15, 16]. The efficiency of gated CMOS GAPD detectors based on single pixels is already known [17, 18]. In this article, we propose the gated mode of acquisition to synchronize the sensor operation with the expected radiation time arrival, reduce the DCP and eliminate afterpulses to increase the efficiency of the detector in CMOS GAPD bidimensional arrays for future linear colliders. In addition, sensor blindness is also avoided.

3 Detector design and operation

The block diagram of the proposed GAPD detector together with the schematic of the pixels is shown in figure 1. The detector consists of an array of 3×3 pixels. It was designed and fabricated with the standard HV-AMS $0.35\mu\text{m}$ CMOS technology (h35b4). Each pixel combines a rectangular GAPD with a sensitive area of $20\mu\text{m} \times 100\mu\text{m}$ and proper readout electronics. Transistor M_R was included to study the response of the detector for different recharge times, achieved through an

external adjustable V_{bias} , but it is not used in the gated mode of operation. It could be removed to minimize the area occupation as well as the charge flowing during an avalanche. The photodiode is implemented by means of a p^+ /deep n-tub junction, which is surrounded by a p-tub implantation set to prevent premature edge breakdown. Additionally, the corners of the sensor are smoothed to avoid electric field peaks at the junction corners. Pixels of rows 0 and 1, and pixels of row 2, share the deep n-tub layer to obtain a reduced pitch ($22.9\mu\text{m}$) and an improved fill factor (90.2%). Reverse bias voltages of $V_{\text{BD}} + V_{\text{OV}}$ (with $V_{\text{BD}} = 18.9\text{ V}$) are applied at the sensor cathode to operate the Geiger mode, while a V_{DD} of 3.3 V powers the rest of the pixel. The readout is performed at the anode or sensing node (V_{S}).

In the GAPD detector proposed in this work, the gated operation is controlled by means of two external signals implemented through MOS transistors. When turned on by the RST signal, transistor M_{N0} quickly recharges the sensor by increasing its bias over V_{BD} and the gated ‘on’ period is started. However, given that avalanches can still happen while the RST transistor is on, the RST pulse has to be as short as possible in order to minimize the presence of low resistive paths from V_{S} to ground and ensure a robust quenching. On the contrary, when the INH signal switches on transistor M_{P0} , the polarization of the sensor is reduced under V_{BD} , defining this way the gated ‘off’ period. When an avalanche is triggered, the self-sustained current that flows through the junction charges the parasitic capacitance (C_{Q}) of V_{S} in picoseconds until its voltage has raised up to V_{OV} . At this point, the polarization of the sensor has dropped down to V_{BD} and the avalanche is quenched. Node V_{S} is connected to the readout electronics, which is based on a level-shifter (M_{P1} , M_{P2} and M_{P3}) and a CMOS inverter (M_{P4} and M_{N1}). Low V_{OV} are desired to reduce the DCR. However, they are not allowed in this technology given that the threshold voltage of nMOS transistors is set at 0.5V. In order to overcome this drawback, a level-shifter biased externally was included to rise the avalanche voltage over the threshold voltage of the following CMOS inverter, which is set at $V_{\text{DD}}/2$. The output of the inverter is feed in a dynamic latch (M_{N2} , M_{P5} and M_{N3}) which has been included to make possible in-pixel storage. The dynamic latch is synchronized with the active periods of the sensor by means of the external signal CLK1. This signal switches on pass gate M_{N2} at the beginning of the gated ‘on’ period and switches it off a few nanoseconds before the gated ‘off’ period is started to avoid storing a false ‘1’. The interval of time in which the dynamic latch is sampling the inverter output is called period of observation (t_{obs}). The value of V_{S} at the end of t_{obs} is stored during the gated ‘off’ period. The gating periods are globally applied to all the pixels simultaneously. The waveforms to control the GAPD in the gated operation are depicted in figure 2.

The three rows of the GAPD array are read sequentially during the gated ‘off’ periods of the sensor. Thereby, the three columns of each row are read in parallel, requiring only three output pads. To allow external selection of the row to be read, a simple address circuit based on a pass gate (M_{N4}) activated by the CLK2_m signal has been placed between the dynamic latch and the output column line. When triggered by CLK2_m (i.e., CLK2_m=‘1’), each one of the selected pass gates feeds its corresponding output column line, which is directly connected to the output pad. Signal reaches the output pad within 2ns time. Despite the small number of pixels, the presented array is a demonstrator of a larger bidimensional camera.

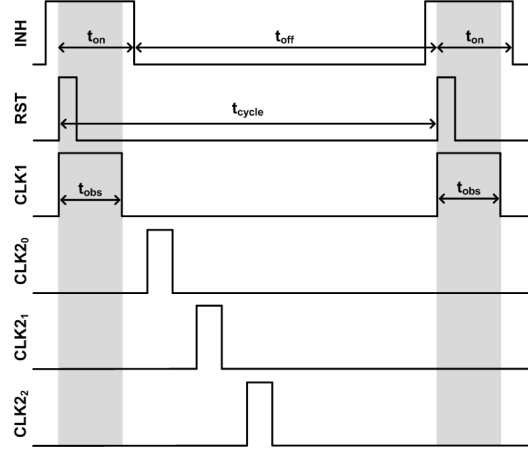


Figure 2. Waveforms for the gated acquisition.

4 Results and discussion

To demonstrate the efficiency of the proposed methods to reduce the noise in GAPD detectors, the response of the pixel in darkness was tested at room temperature. The chip was mounted on a printed circuit board and powered with an Agilent E3631A voltage source. An Altera Stratix II FPGA-based control board was used to generate the fast logic control signals (RST, INH, CLK1 and CLK2_m) and also to count off-chip the number of pulses generated by the sensor. The measurements were done with an adjustable integration time that depends on the period of observation of the sensor and also on the number of times that the observation is repeated (n_{rep}). Different t_{obs} that range from 10ns to 1280ns were analyzed for different V_{OV} .

Firstly, the afterpulsing probability was tested by leaving different gated ‘off’ periods for a fixed t_{obs} of 10ns. It was observed that gated ‘off’ periods of 300ns are enough to eliminate afterpulses at 1.0V of V_{OV} [18], which shows that the lifetime of the trapping levels is shorter than this time. In fact, gated ‘off’ periods of GAPD arrays for ILC experiments can be almost equal to the interbunch spacing (337ns) to eliminate afterpulses while synchronizing the detector performance with the beam timing. In addition, the gated ‘off’ periods of the sensor can be also used to sequentially read out the in-pixel stored information row by row. A completely different scenario occurs at CLIC. Given the extremely high BX rate, it would be impossible to get rid of afterpulses before the next BX takes place, leaving no choice but to live with it.

Secondly, the dark counts of the detector were characterized for two different V_{OV} (1.0V and 1.5V) and several t_{obs} (from 10ns to 1280ns) with a fixed t_{off} of 300ns (figure 3). In order to obtain a statistical population, $4 \cdot 10^5$ repetitions of each point of the experiment were performed. As expected, the dark counts are reduced for a lower V_{OV} . Moreover, they are linearly decreased with shorter t_{obs} . The pixels present the same relative count rate change with t_{obs} . Given that the DCR is a random phenomenon, if the sensor is active only during short discrete intervals in the nanosecond range, the probability to observe a dark count is reduced. In addition, since the gated acquisition also allows to synchronize the active periods of the sensor with the expected signal arrival, no events will be lost. We can conclude that the gated acquisition is an effective technique to reduce the probability to observe the noise in GAPDs.

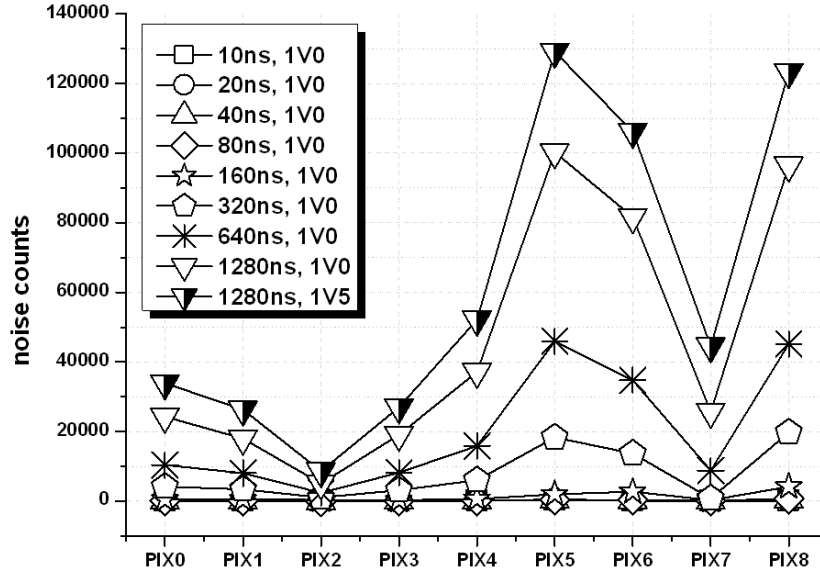


Figure 3. Noise counts of the different pixels for the array for different t_{obs} and V_{OV} .

In figure 3 it can also be observed that the increase of the noise counts shows a similar behaviour amongst the different pixels of the array as t_{obs} is widened. However, noise discrepancies in absolute values for the different pixels are large, as it usually happens in GAPD arrays [9]. There is a significant variation of a factor 20 between the most and the less noisy pixels, which are PIX5 and PIX2, respectively. PIX6 and PIX8 present similar variations with respect to PIX2. The rest of the pixels of the array show variations from a factor 3 up to a factor 5 regarding PIX2. These noise discrepancies may lead to an irregular detector performance, in which high noisy pixels (dead pixels) are always fired by the noise and contribute to sensor blindness. In order to prove the efficiency of the gated acquisition in terms of avoiding sensor blindness, we propose one last experiment. The response of the detector was analyzed for two different t_{obs} of 10ns and 10 μ s with a V_{OV} of 1V (figure 4). In the 10 μ s case, almost all the pixels are fired by a dark count. In this situation, the GAPD detector is blind because of the noise and no detection is possible. This is not the case for short t_{obs} of 10ns, in which all the pixels are ready to detect signal. This experiment proves that the gated operation is efficient in avoiding sensor blindness in triggered systems.

The gated acquisition can also increase the efficiency of GAPD detectors in ILC and CLIC, as it will be explained. At ILC, when the sensor is operated in the free running mode, 9.503 noise counts/pixel/train are assumed to happen (where $\text{noise counts}_{\text{pixel}} = \text{DCR}_{\text{pixel}} \cdot \text{bunch train period}$, $\text{DCR}_{\text{pixel}} = 10\text{kHz}$ and bunch train period = $2820\text{BXs} \cdot 337\text{ns} = 9.5 \cdot 10^{-4}\text{s}$). This implies that the sensor is blind because of the noise and no detection is possible. In contrast, when the sensor is operated in the gated mode with short t_{obs} periods, the expected noise can be reduced down to 0.282 noise counts/pixel/train with a t_{obs} of 10ns and to 0.056 noise counts/pixel/train with a t_{obs} of 2ns. This confirms that the gated acquisition is an effective technique in reducing noise figures and avoiding sensor blindness. Apart from that, given the accurate time response of GAPDs and the speed of the standard HV-AMS 0.35 μm CMOS technology, it is possible to read the detector after each BX. In addition, it is also possible to time-stamp the pixel data to distinguish events in different

(1) $t_{\text{obs}}=10\mu\text{s}$, $n_{\text{rep}}=1$				(2) $t_{\text{obs}}=10\text{ns}$, $n_{\text{rep}}=1$			
noise counts							
	1	0	0	0	0	0	
	1	1	1	0	0	0	
	1	1	1	0	0	0	

Figure 4. Noise counts of the GAPD array for one repetition of the active period of the sensor for two different t_{obs} : $1\mu\text{s}$ (1) and 10ns (2).

BXs. At CLIC, the sensor can be operated in the gated acquisition with an active period equal to the length of the entire train. In this case, $1.5 \cdot 10^{-3}$ noise counts/pixel/train are expected, where the bunch train period is calculated as $312\text{BXs} \cdot 0.5\text{ns} = 1.56 \cdot 10^{-7}\text{s}$. However, considering the expected hits at ILC [1] and CLIC [2], the performance of the detector is still unsatisfactory because the signal-to-noise ratio is low. Further solutions have to be studied. For instance, another conventional technology with a lower DCR could be used to reduce the intrinsic noise of the sensor. The mean DCR of the standard HV-AMS $0.35\mu\text{m}$ CMOS technology (measured to be 10kHz) is a very high value, yet mean DCRs as low as 50Hz and 10Hz have been reported with a $0.8\mu\text{m}$ CMOS standard technology [9] and a 130nm CMOS standard technology especially modified for GAPDs [10], respectively. In addition, to further reduce the number of observed dark counts, the active periods of the sensor could be decreased below the nanosecond by monolithically integrating a control signal generation circuit. Moreover, data processing from different layers of the detector would make possible to distinguish real events from noise counts. In fact, a structure of double layers is already planned for CLIC. Hits from a first layer without their corresponding hit in a second layer cannot form feasible traces and must therefore be discarded, thus eliminating noise counts.

5 Conclusion

A GAPD bidimensional array that can be operated in the gated mode has been fabricated with the $0.35\mu\text{m}$ HV-AMS standard technology for future linear colliders. The proposed detector is the only current candidate that is fast enough to allow single BX detection at ILC and also could handle with CLIC timings. It has been demonstrated that the gated operation with long enough gated ‘off’ periods allows to eliminate the afterpulsing probability. Short gated ‘on’ periods with low reverse

overvoltages minimize the dark count probability. We can conclude that the gated acquisition with short t_{obs} in the nanosecond range allow to highly improve the detector efficiency and avoid sensor blindness. However, further studies have to be considered in order to avoid the noise masking the signal.

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