Optimization of KOH etching process to obtain textured substrates suitable for heterojunction solar cells fabricated by HWCVD

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Abstract

In this work, we have studied the texturization process of (100) c-Si wafers using a low concentration potassium hydroxide solution in order to obtain good quality textured wafers. The optimization of the etching conditions have led to random but uniform pyramidal structures with good optical properties. Then, bifacial heterostructures were fabricated by Hot-Wire CVD onto these substrates and the Quasi-Steady-State PhotoConductance technique was used to measure passivation quality. Little degradation in the effective lifetime and implicit open circuit voltage of these devices (<20 mV) was observed in all cases. It is especially remarkable that for big uniform pyramids, the open-circuit voltage is comparable to the values obtained on flat substrates.

Keywords

Hot-Wire deposition, Solar cells, Heterostructures, etching.

Introduction

Heterojunction solar cells consisting of hydrogenated amorphous silicon (a-Si:H) films deposited on crystalline silicon (c-Si) wafers have attracted the interest of the photovoltaic community due to their high-efficiency and cost effective fabrication process [1]. The main advantage of heterojunction solar cells is that no high temperature steps are required to form the junction of the device, allowing the possibility of costs saving through the use of thinner and lower grade Si wafers. In heterojunction solar cells, accurate control of the a-Si:H/c-Si interface becomes an important factor for high performance. For simplicity, most groups have started their research in heterojunction solar cells using flat substrates. However, the situation differs significantly on textured substrates where pyramids a few microns high have to be covered by conformal thin films only some tens of nanometre thick. Moreover, the crystalline orientation (111) in textured substrates instead of the usual (100) of flat substrates can also have significant influence in interface passivation. Actually, special attention to wet-chemical pre-treatments is required to assure a low interface defect density on textured substrates [2]. Apart from Sanyo, only a few groups have succeeded fabricating high efficiency bifacial heterojunction solar cells on textured wafers [3, 4]. In general, the expected increase in the short circuit current density (J_{sc}) is partially counterbalanced by a lower V_{oc} value compared to devices on flat substrates [5].

Silicon wafer random texturing is usually achieved in commercial solar cells by an anisotropic etching of the silicon network. Although dry etching techniques are currently under investigation, wet etching by an alkaline solution is the standard process for industrial solar cell texturing. In fact, wet chemical etching is also routinely used in crystalline silicon cell processing to remove sawing damage. The most widely used anisotropic etching is a low concentration potassium hydroxide (KOH) solution in water

with the addition of isopropyl alcohol (IPA). This has been the approach used in this work to obtain textured wafers with different pyramid configuration. These substrates have been used to study surface passivation with thin a-Si:H films deposited by Hot-Wire CVD of textured wafers. Since our group has already obtained good results in heterojunction solar cells on flat substrates [6], this work aims to increase the J_{sc} value without a significant V_{oc} loss.

Experimental

All the heteroestructures presented in this work were obtained on CZ silicon wafers with (100) crystalline orientation, thickness around 350μm and p-type resistivity of 2.6 Ωcm. Before the texturization process, silicon wafers were cleaned in a H_2SO_4:H_2O_2 (2:1) solution. Then, they were dipped in 5% HF until they become hydrophobic. Substrates with randomly distributed upside pyramids were prepared by anisotropic etching of Si using a low concentrated alkaline (KOH) - Isopropanol (IPA) solution. The etching process has been widely studied performing experiments varying the most significant parameters (temperature, IPA and KOH concentrations) to obtain different pyramid configuration. The etching set-up consisted in a capped vessel with a reflux condenser to prevent the loss of chemical during the texturization process and a hot plate stirrer with an optimised PID control with a stainless steel sensor for the temperature.

The morphology of all the samples was characterized by means of SEM images and reflectance measurements. The reflectance set-up consisted in a Spectrophotometer with an integration sphere Perkin Elmer Lambda 19 (300-2000nm). To calculate the etching rate, we have weighted the samples before and after the etching process.

Before the intrinsic a-Si:H layers deposition, silicon wafers were cleaned in a two step wet chemical procedure. First, a previous RCA II was done to remove the K^+ from the c-Si surface. After, all the substrates were cleaned in a complete RCA [7] just before their introduction into our ultra-high vacuum deposition system. All the intrinsic thin silicon films were grown by HWCVD under the deposition conditions summarized in table I. Two parallel tantalum wires (∅ = 0.5 mm) separated 3 cm have been installed for better uniformity, with the gas inlet centred 1 cm below the wires. The substrate is placed 4 cm above the plane of the wires.

The effective lifetime (τ_{eff}) as a function of the average excess minority carrier density (Δn) was measured by the contactless Quasi-Steady-State Photoconductance (QSS-PC) technique [8]. The QSS-PC data implicitly contain information about the open-circuit voltage expected from the solar cell precursor. For instance, considering a solar cell on a p-type wafer with acceptor density N_A, the expected V_{oc} value would be given by:

$$V_{oc} = \frac{kT}{q} \ln\left[\frac{\Delta n(N_A + \Delta p)}{n_i^2} + 1\right] \quad (1)$$

Results & Discussion

In this work, we have started studying the surface morphology of the different samples obtained varying the texturization process. We have maintained constant the %wt of KOH to very low values (5%), as an industrial requirement for mass production solar cells. Then, we have varied the temperature and the %vol IPA as they are the most critical parameters [9]. Figure 1 shows the influence of both the %vol IPA and the temperature on the etching rate. The most important conclusion is the strong dependence of the etch rate on the IPA concentration. In addition, the size of the pyramids basis decreases for higher IPA

concentrations. It is well known that IPA can pollute the workshop and is the most expensive part of the process [10] [11], so one of the most interesting trends is to reduce the IPA concentration. Hence, the optimum concentration of IPA will be the lowest to assure the uniformity of the surface with a high etching rate. On the other hand, the temperature also plays an important role. Contrarily to the IPA concentration, the etching rate increases with the temperature to a stabilized value for temperatures over 85ºC.

Then, varying these two parameters we have optimized the conditions to obtain different pyramid configurations. The four different pyramid patterns obtained on (100) silicon wafers are summarized in table II with their corresponding etching conditions. A flat polished sample labelled F has been used as a reference. The morphologies of three of these samples are shown in figure 2. In T1 large flat zones are present in the sample, while for T2 and T4 the complete surface is covered by pyramids in a random structure. The height of the pyramids in T2 and T4 ranges between 2-9 μm and 3-15 μm, respectively.

In order to study the optical confinement, the reflectance of the textured samples was compared to a reference flat wafer (figure 3). When using a pyramid texture a double rebound against the surface is expected though decreasing the whole measured reflectance. Thus, in an ideal case, the minimum measured reflectance for this specific pyramid texture should be around (R_F^2), where R_F is the reflectance measured by the flat wafer. R_F^2 is also represented in figure 3 (dashed line) and it is clearly observed that the measured values for T2 and T4 are very close to this optimum value. By contrast, the reflectance measured for the T1 is higher due to the presence of the flat zones in which the antireflection effect is not present. Then, from an optical point of view the texturization of samples T2 and T4 is sufficient to get and optimum antireflection effect.

Next, intrinsic a-Si:H layers were deposited by HWCVD on all the samples. The QSS-PC measurements are shown in figure 4. The passivation quality is worse for the sample with

isolated pyramids (T1) and then steadily increases to a value comparable to the reference sample (implicit V_{oc}=650mV) for high pyramids (T4). As observed in the SEM images, the sample T1 presents non-textured areas and first-stage pyramids dealing to an irregular surface. Hence, this rough morphology could result in a high surface state density having direct detrimental effect in the passivation quality.

It has been reported [2] the importance of the cleaning procedure between the KOH etching and the a-Si:H deposition to obtain a good interface for heterojunction devices. In this sense, the double RCA cleaning performed in our textured samples has led to a very clean interface. It is also worthy remarking the case with bigger pyramids (average 10 μm basis) with implicit V_{oc} values similar to the flat reference. In fact, the interface state density of (111) orientation can be as low as for (100) after an adequate wet pre-treatment [2]. Considering that the effective passivated surface is higher for textured wafers, we can conclude that an excellent passivation quality has been achieved with intrinsic a-Si:H films obtained by HWCVD. This is an encouraging result for the fabrication of heterojunction solar cell over textured substrates by HWCVD.

Conclusions

In this work, we have studied the texturization process of (100) c-Si wafers using a KOH anisotropic etching. The optimization of the process has lead to random but uniform pyramidal structures with excellent optical properties. The passivation results with HWCVD intrinsic a-Si:H layers show little degradation in the implicit V_{oc} (<20mV) in all cases. In particular, for high size pyramid textures we have achieved a passivation quality similar to the flat reference.

Acknowledgments

This work has been supported by the Spanish Government through the projects CLASICO (ENE2007-67742-C04) and PSE-MICROSIL08.

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Table I: Deposition conditions for the HWCVD intrinsic a-Si:H layers used in this work.

Figure 1: Dependence of the etching rate on the IPA concentration and the solution temperature.

Table II: Etching conditions used in this work for the different pyramid configurations.

Figure 2: SEM images of the random pyramids obtained for three of the samples considered in this work (T1, T2 and T4).

Figure 3: Reflectance measurements for the samples under study compared with the flat substrate and minimum reflectance considering the double rebound effect (R_F^2).

Figure 4: Implicit-V_{oc} (columns) and effective lifetime (squares) measured by QSS-PC for the passivated reference and textured substrates.

Type	T_s (ºC)	H_2 (sccm)	SiH_4 (sccm)	P (mbar)	T_f (ºC)	r_d (Å/s)
intrinsic	200	-	4	1×10^{-2}	1600	5

Table I

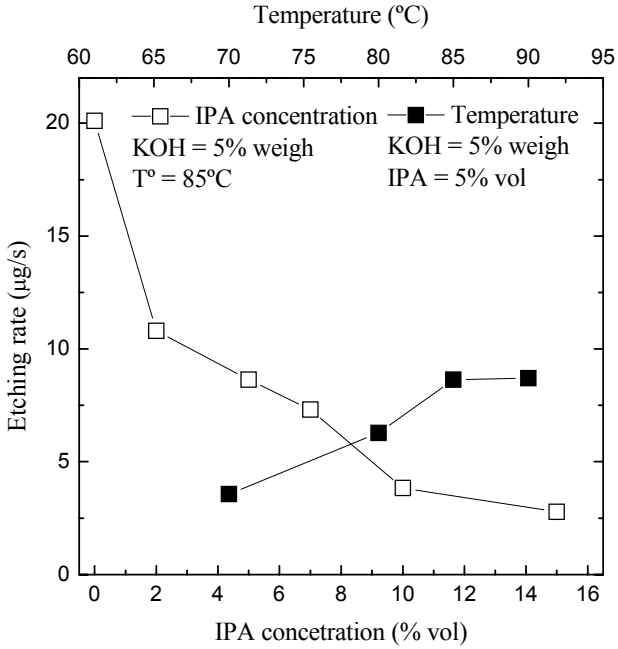
Temperature (ºC)
60
65
70
75
80
85
90
95
IPA concentration
KOH = 5% weigh
Tº = 85ºC
Temperature
KOH = 5% weigh
IPA = 5% vol
Etching rate (µg/s)
0
5
10
15
20
0
2
4
6
8
10
12
14
16
IPA concetration (% vol)

Figure 1

Sample	KOH %wt	IPA %vol	Tª ºC	t min	Remarks
T1	5	5	85	10	Small non-uniform
T2	5	5	80	60	Small uniform
T3	5	5	85	60	Medium uniform
T4	5	7	90	60	Big uniform
F	-	-	-	-	Flat polished

Table II

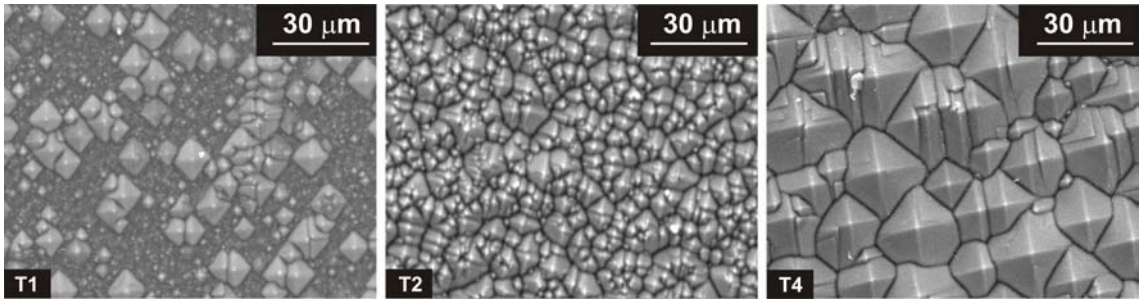

Figure 2

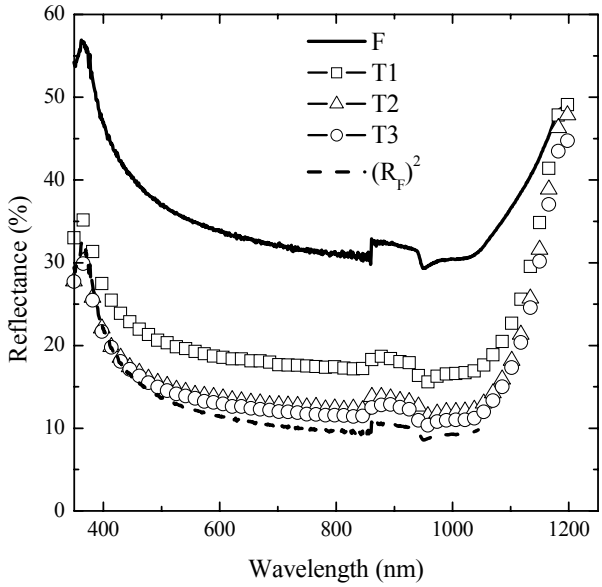
F
T1
T2
T3
$\cdot(R_F)^2$
Reflectance (%)
Wavelength (nm)
0
10
20
30
40
50
60
400
600
800
1000
1200

Figure 3

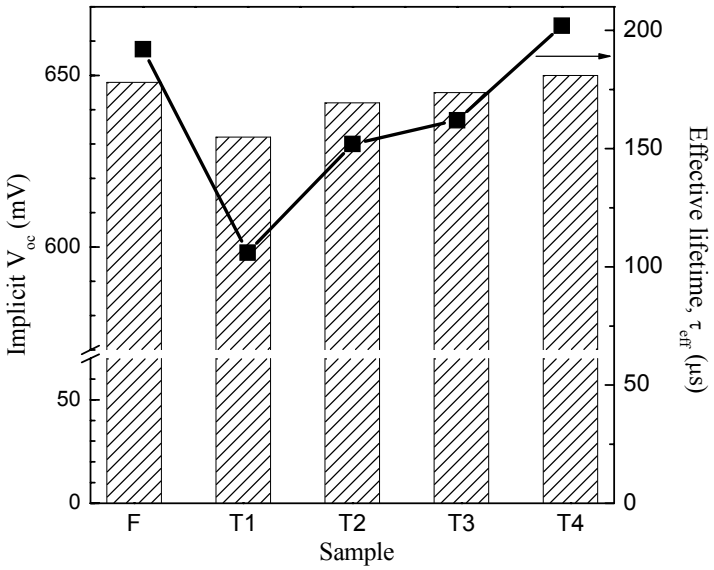
650
600
50
0
200
150
100
50
0
F
T1
T2
T3
T4
Sample
Implicit V_{oc} (mV)
Effective lifetime, τ_{eff} (μs)

Figure 4