ELECTRONIC TRANSPORT IN LOW TEMPERATURE NANOCRYSTALLINE SILICON THIN-FILM TRANSISTORS OBTAINED BY HOT-WIRE CVD

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Abstract

Hydrogenated nanocrystalline silicon obtained by Hot-Wire Chemical Vapour Deposition has been incorporated as the active layer in bottom-gate thin-film transistors. These devices were electrically characterised by measuring in vacuum the output and transfer characteristics for different temperatures. The field-effect mobility showed a thermally activated behaviour which could be attributed to potential barriers for the electronic transport. Trapped charge at the interfaces of the columns, which are typical in hydrogenated nanocrystalline silicon, would account for these barriers. By using the Levinson technique, the trapped charge density at the column boundaries is estimated. Finally, these results are interpreted according to the particular microstructure of this material.

1. Introduction

The Hot-Wire Chemical Vapour Deposition (HWCVD) technique has shown its ability to obtain hydrogenated amorphous and nanocrystalline silicon thin-film transistors (TFT) at low substrate temperatures (<200 ºC) with acceptable field-effect mobilities and threshold voltages [1,2]. Besides, improved stabilities of these devices compared to their counterparts deposited by Plasma-Enhanced Chemical Vapour Deposition

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(PECVD) have been reported [3]. In this work we report on the electronic transport properties of hydrogenated nanocrystalline silicon (nc-Si:H) obtained by HWCVD at low substrate temperatures (150ºC) from electrical measurements on field-effect structures. The usual columnar microstructure of nanocrystalline silicon films suggests that the coplanar electronic transport is mainly determined by the column boundaries [4]. Hence, the field-effect mobility (μ_s) of nanocrystalline silicon TFTs would allow us to obtain information about the quality of the material between the columns. In this work we have measured the thermal dependence of the field-effect mobility for different gate-source voltages. These results were interpreted considering potential barriers at the interface between columns due to trapped charge therein. This model allowed us to explain the thermally activated behaviour of the field-effect mobility by considering that the electronic transport is limited by the thermionic emission of carriers over the barrier[5].

2. Experimental

Hydrogenated nanocrystalline silicon thin-film transistors were deposited by HWCVD in an ultra-high-vacuum multichamber set-up described elsewhere[6]. The gas mixture consisted of 4 sccm of silane diluted into 76 sccm of hydrogen. It was catalytically dissociated by a tungsten wire heated to 1700 ºC at a process pressure of 3.5×10^{-2} mbar. The substrate temperature was only 150 ºC. The resulting deposition rate was around 10 Å/s. These films were grown on a thermally oxidised n-type (100) silicon wafer (1-10 Ωcm) to fabricate bottom-gate thin film transistors (figure 1). The thicknesses of the SiO_2 gate dielectric and the active layer were both around 250 nm. The top n-doped layer (50 nm) was also deposited by HWCVD whereas the source and drain contacts were obtained by thermal evaporation of a chromium layer in high vacuum. The thin-film transistors were defined by photolithography. The width of the channel (W) was

140 μm and its length (L) 10 μm for an aspect ratio (W/L) of 14. The electrical properties of the TFTs were measured under vacuum in dark conditions by means of a semiconductor parameter analyser (Hewlett Packard 4145B) and a programmable temperature controller (MMR Technologies K-20).

3. Results

The transfer characteristic of the studied nc-Si:H thin-film transistor is shown in figure 2. Drain currents (I_D) over microamperes could be easily obtained for moderated gate-source voltages (V_{GS}) with a drain-source voltage (V_{DS}) of only 1 V. The relatively high off-current in the order of a few hundreds of picoampers is due to the high bulk conductivity of the nc-Si:H active layer. The inset shows the output characteristic of the same device. Neither current crowding for low drain-source voltages (V_{DS}) nor kink effect for higher V_{DS} values were observed. This indicates a low contact resistance at the source and drain electrodes with a low carrier injection. Satisfactory drain-source saturation currents in the range of several tens of microamperes could be obtained.

On the other hand, the field-effect mobility (μ_s) and the threshold voltage (V_t) can be obtained from the saturation characteristic (V_{GS}=V_{DS}). Then, I_D can be approximated by the following equation:

$$I_D = \frac{W}{L}\mu_s C_i \frac{1}{2}(V_{GS} - V_t)^2 \qquad (1)$$

where W/L is the aspect ratio of the TFT and C_i the capacitance of the insulator per unit area. Thus, a linear fit to the $\sqrt{I_D}$ vs. V_{GS} plot (figure 3) leads to a negative threshold voltage of –2.0±0.2 V with an average field-effect mobility of 0.50±0.02 cm^2/Vs.

By differentiating equation (1) the field-effect mobility as a function of V_{GS} can be obtained. In figure 4 it is observed a steady increase in μ_s for higher V_{GS} values together with a thermally activated behaviour (equation 2)

$$\mu_s = \mu_o \exp\left(\frac{-E_a}{kT}\right) \tag{2}$$

The corresponding activation energy (E_a) could be related to the height of potential barriers due to trapped charge at the interfaces between columns[7]. The obtained barrier heights ranged from 80 to 70 meV (inset of figure 4). The slight lowering of the barrier with the gate-source voltage could be caused by the screening due to a higher carrier density. The column boundaries can be studied by using the Levinson technique [8]. From a fit to $ln(\ I_D / V_{GS}\ )$ vs. $1 / V_{GS}$ in the linear region (figure 5), the density of charged states at the column boundaries (N_T) is estimated by using the following relation

$$\frac{I_D}{V_{GS}} = \frac{W}{L}\mu_o V_{DS} C_i \exp\left(-\frac{e^3\ N_T^2\ d}{8\,\varepsilon\,kT\,C_i}\frac{1}{V_{GS}}\right) \tag{3}$$

where d is the thickness of the active layer and N_T the density of charged states at the column boundaries. This equation is valid for high V_{GS} values, when the electron concentration within the channel is larger than a critical value $N_T/2r$, where r is the mean radius of the columns [8]. Then, the density of charged states at the column boundaries can be estimated in around $3.0\pm0.5\times10^{11}$ cm^{-2}.

4. Discussion

Structural characterisations suggest that the studied nanocrystalline silicon films consist of crystallites of a few nanometers embedded into columns with a typical radius of several tens of nanometers (~50 nm). Although structural characterisations, such as

Raman spectroscopy or X-ray diffraction, detect crystallographic grain sizes of just a few nanometers[9], Scanning Electron Microscopy (SEM) images of our samples evidenced a microstructure consisting of columns with a mean radius around 50 nanometers. Average crystallite sizes of a few nanometers would lead to crystallite densities over 10^{18} cm^{-3}. Hence, to form potential barriers there had to be more than 10^{18} cm^{-3} electrons trapped at the grain boundaries. These densities are unlikely for the undoped nc-Si:H layers under study. For that reason, some authors have discarded the possibility of potential barriers at the grain boundaries of crystallites as the main mechanism determining the electronic transport in nc-Si:H films [10]. However, the field-effect mobility of our TFTs which incorporated undoped nc-Si:H layers showed a thermally activated behaviour (figure 4). This suggests that potential barriers could exist at structures bigger than the crystallites. According to previous works[11], we assume that potential barriers exist not at the grain boundaries of crystallites but at the interfaces between columns. Then, considering that the columns have an average diameter of several tens of nanometers, less than 10^{17} cm^{-3} trapped carriers would be sufficient to form potential barriers. This agrees with the subgap optical absorption measured by photothermal deflection spectrometry, which roughly estimates a deep level density in the range of 10^{17} cm^{-3}. In the same trend, capacitance-voltage measurements of Schottky contacts also pointed to trapped charge densities of the order of 10^{17} cm^{-3} within the space charge region. We think that these densities are mainly due to dangling bonds at the boundaries between columns.

Finally, if we consider cylindrical columns of radius r, the surface density of states (N_S) could be related to the volume density of states (N_V) by the following equation:

$$N_V \approx \frac{2\pi r d}{\pi r^2 d} N_S = \frac{2}{r} N_S \qquad (4)$$

where d is the column height, i.e., the film thickness. From equation (4), a typical N_V value in the range of 10^{17} cm^{-3} leads to an N_s value of the order of 10^{11} cm^{-2} for the mean radius of 50 nm determined by SEM. This N_s value agrees with the density of charged states at the column boundaries estimated by the Levinson technique in the previous section.

5. Conclusions

The study of the electronic transport parallel to the substrate is a main subject to elucidate the suitability of the nc-Si:H material in thin-film transistors. Results suggest that potential barriers at the boundaries between columns could limit the field-effect mobility of these devices. The thermally activated behaviour of the field-effect mobility could be explained by barrier heights around 80 meV which slightly decrease with the gate-source voltage. These barriers could be attributed to trapped charge at the interfaces between the columns. The density of charged states at the column boundaries was estimated in around $3.0\pm0.5\times10^{11}$ cm^{-2} by the Levinson technique. Lower densities of charged states at the interfaces between columns would reduce the barrier height and consequently increase the field-effect mobility values.

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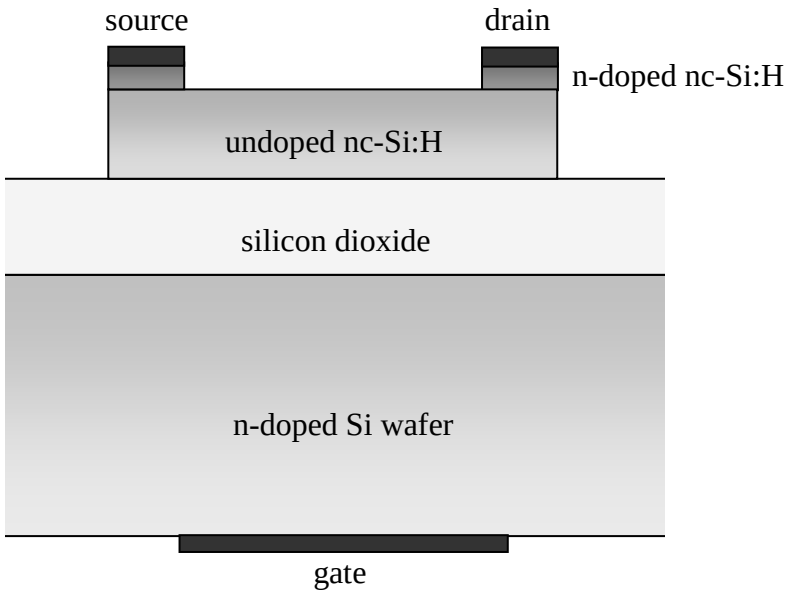
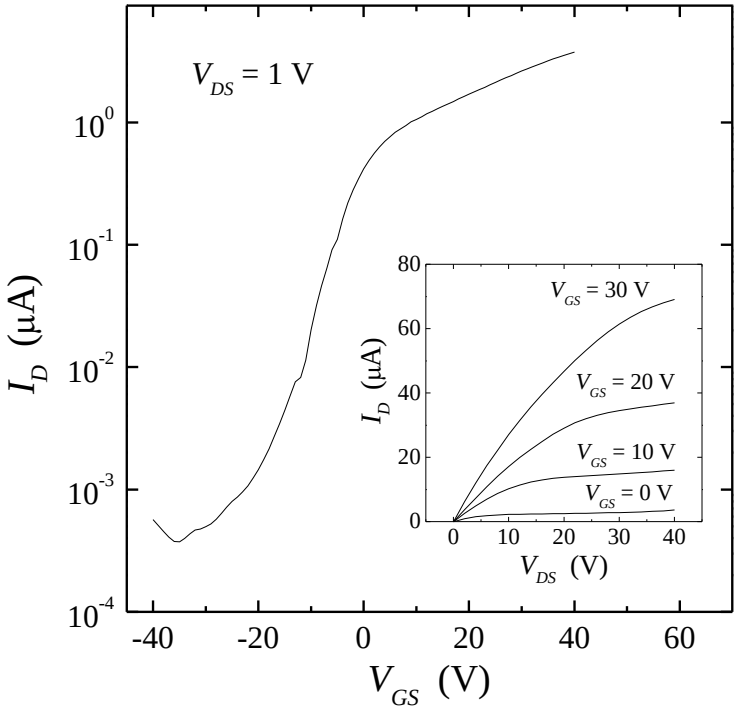


Figure 1. J. Puigdollers et al.



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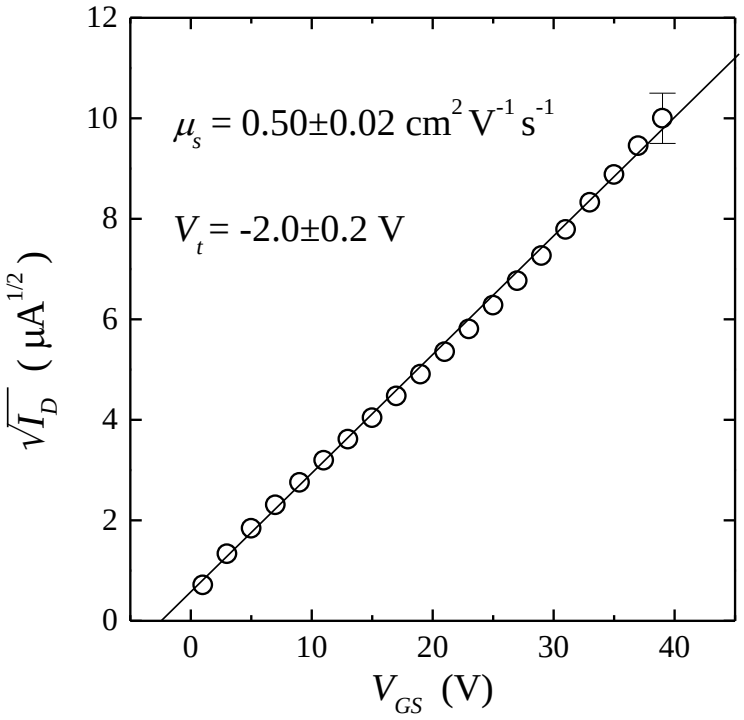

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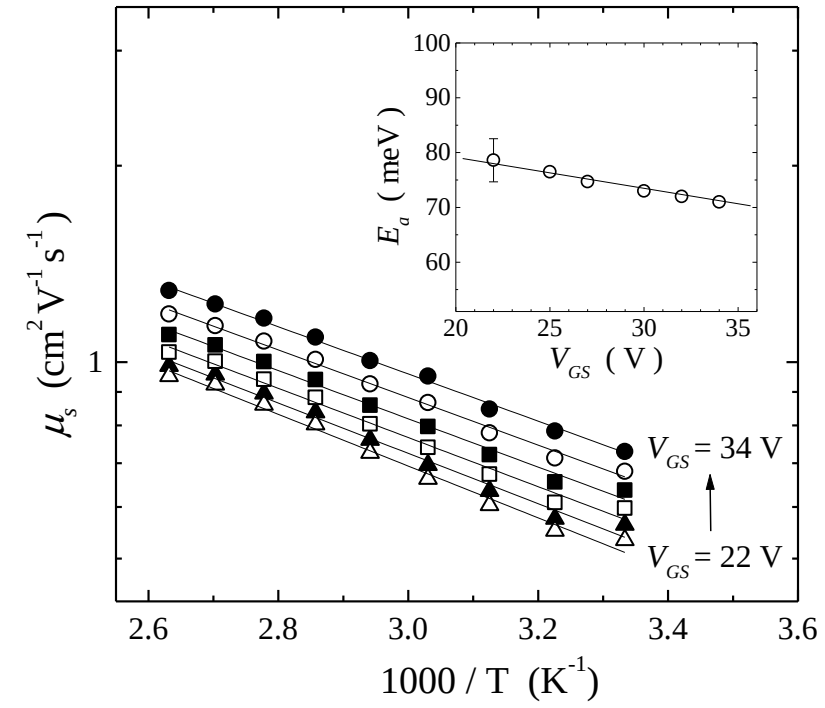

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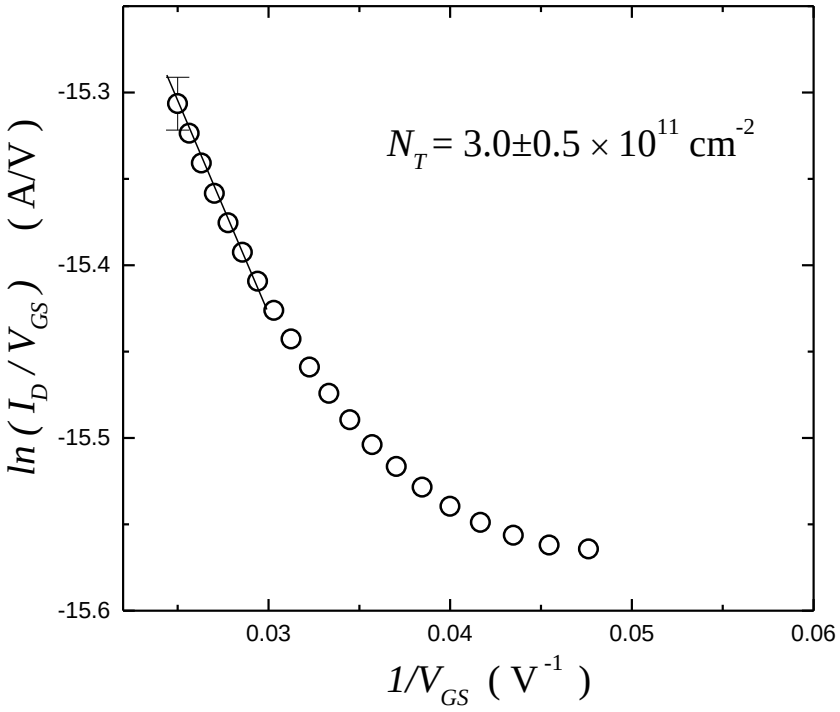

Figure 5. J. Puigdollers et al.