Low temperature amorphous and nanocrystalline silicon thin film transistors deposited by Hot-Wire CVD on glass substrate

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Abstract

Amorphous and nanocrystalline silicon films obtained by Hot-Wire Chemical Vapor deposition have been incorporated as active layers in n-type coplanar top gate thin film transistors deposited on glass substrates covered with SiO₂. Amorphous silicon devices exhibited mobility values of 1.3 cm²V⁻¹s⁻¹, which are very high taking into account the amorphous nature of the material. Nanocrystalline transistors presented mobility values as high as 11.5 cm²V⁻¹s⁻¹ and resulted in low threshold voltage shift (~ 0.5 V).

Keywords

Thin film transistor, Amorphous and nanocrystalline silicon, Hot-Wire CVD
1. Introduction

Nowadays, the electronic devices used to process the signal given by mechanical, chemical or biological functions need to be made on the same substrate used for these other functions. In many cases, the substrate is a glass or a plastic that does not support high temperatures. In particular, thin film transistors (TFTs) are widely used as active elements in active-matrix liquid crystal displays (AMLCDs) applications in flat panel displays (FPDs) like portable laptop computers, mobile phones and personal digital assistants (PDAs) [1].

This need to obtain TFTs at low substrate temperatures has drawn the attention to silicon deposition techniques like Hot-Wire Chemical Vapor Deposition (HWCVD), as they allow device-quality material deposition of both amorphous (a-Si:H) and nanocrystalline (nc-Si:H) silicon thin films at substrate temperatures (T_s) below 300°C. Using higher substrate temperatures, mobilities (µ) of around 0.7 cm²V⁻¹s⁻¹ for a-Si:H [2] and 1.4 cm²V⁻¹s⁻¹ for heterogeneous silicon (het-Si:H) [3] both deposited by HWCVD have been shown in bottom gate structures. Regarding nc-Si:H, mobility values as high as 40 cm²V⁻¹s⁻¹ have been reported for staggered top gate bottom source/drain geometry using Very High Frequency (VHF) Plasma Enhanced CVD (PECVD) at 150°C [4].

In this paper we focus on the fabrication of coplanar top gate TFTs based on HWCVD a-Si:H and nc-Si:H deposited on SiO₂ coated glass.

2. Experimental

Top gate TFTs have been processed using 200 nm-thick a-Si:H or nc-Si:H silicon films deposited by HWCVD in a multichamber deposition set-up described elsewhere [5] on 2×2 square inch glass substrates covered with 200 nm Atmospheric Pressure CVD (APCVD) deposited SiO₂. a-Si:H has been deposited at a filament temperature (T_f) of around 1680°C, a substrate temperature of 200°C, process pressure (P) of 1·10⁻² mbar and without any hydrogen dilution (D_H), whereas slightly lower filament temperature (T_f ~ 1610°C), P = 3·10⁻² mbar and D_H = 95% (4 sccm SiH₄ and 76 sccm H₂) were used in the case of the nc-Si:H layers. A 150 nm-thick n-type nc-Si:H layer was deposited on top of the a-Si:H or nc-Si:H layer by adding PH₃ to the gas mixture so that [P]/[Si] was 2% in the gas phase (the rest of the deposition conditions
were the same as those of undoped nc-Si:H). In amorphous TFTs, undoped a-Si:H and n-type nc-Si:H layers were deposited in different chambers, whereas in the case of nc-Si:H ones, deposition of all HWCVD layers took place in the same chamber, just closing the shutter a few seconds to avoid the pressure peak upon the inclusion of PH3 in the gas mixture.

The previous stack of undoped and doped films was processed to fabricate n-type TFTs in the configuration presented in Fig. 1. The doped nc-Si:H layer was plasma etched to define channel, source and drain regions for each transistor. Then, a 100 nm-thick SiO2 layer was deposited by RF sputtering to ensure the gate insulation.

The gate insulator fabrication is, therefore, the most critical step that determines the success of the TFT process. Particularly, it is very difficult to obtain high quality gate insulators at low temperature. Deposition and treatment conditions have been optimized to lead to RF sputtered SiO2 film with gate insulator quality. It was deposited using an Ar/O2 mixture and without heating the substrate holder, so the temperature reached by the film during deposition was around 80ºC. Metal-SiO2-Si capacitances processed using the present silicon dioxide showed a flat-band voltage of -0.2 V and an interface state density D_i = 6.4·10^{10} \text{eV}^{-1}\text{cm}^{-2}. These values are given here to show the high quality of the silicon dioxide and the SiO2/Si interface.

After SiO2 deposition, source and drain contacts were opened through the gate insulator. Finally, aluminum was thermally evaporated and wet etched to form source, drain and gate electrodes. Post-metallization annealing was performed at 200ºC in an atmosphere of forming gas.

TFTs with different channel length (L) and width (W) were simultaneously fabricated. L varied from 20 to 80 µm and W between 20 and 100 µm. TFTs were characterized at 25ºC and then the usual device parameters were determined: threshold voltage (V_T), transconductance (g_m), field effect mobility (\mu) and inverse subthreshold slope (S). V_T and g_m were deduced in the linear regime (low drain-source voltage, V_DS),

$$I_{DS} = \mu \frac{W}{L} C_{ox} V_{DS} (V_{GS} - V_T)$$

(1)

where V_T is the intercept of the transfer characteristics (I_{DS}(V_{GS})) with the gate voltage (V_{GS}) axis, and g_m is the slope of the linear fit. \mu is then deduced from the relation:
\[ \mu = g_m \cdot (L/W) \cdot (1/C_{ox}) \cdot (1/V_{DS}) \]  

(2)

where \( C_{ox} \) is the gate oxide capacitance per area unit, \( C_{ox} = (\varepsilon_0 \varepsilon_{ox})/t_{ox} \), being \( t_{ox} \) the oxide thickness. \( S \) is the inverse slope of the transfer characteristics using logarithmic plot. Finally, stress experiments were performed using a negative gate voltage of -10 V.

3. Results and discussion

3.1. Material characterization

Fig. 2 shows the Raman spectra of two silicon samples (a-Si:H and nc-Si:H) deposited at the same conditions as the ones used in the TFTs under study. In the case of the nc-Si:H layer, a crystalline fraction (\( X_c \), calculated as the weight of the crystalline contribution (520 cm\(^{-1}\)) in the Raman spectra) of approximately 0.50 was measured in a 400 nm-thick layer (thicker than those used in the studied TFTs). When implemented to completely Hot-Wire deposited p-i-n nc-Si:H solar cells, this material has led to stable devices [6].

Regarding the n-type doped material, characterization of a 40 nm-thick n-layer grown in the above-mentioned conditions resulted in a dark conductivity (\( \sigma_d \)) of 5 \( \Omega^{-1}\text{cm}^{-1} \), an activation energy (\( E_a \)) of 0.02 eV and \( X_c = 0.43 \).

3.2. a-Si:H TFTs

Fig. 3 shows the typical transfer characteristics of the amorphous silicon TFTs. It is clear from this curve that both \( S \) and \( V_T \) were low, thus ensuring a fast transition between the “on” and “off” states. Table 1 summarizes the mean parameters deduced from the characteristics of about thirty TFTs.

The determined values confirm the first observation of the transfer characteristics. Moreover, the mobility value can be considered as very high for a-Si:H devices if we compare them with values commonly found in literature [1,2]. This result is very interesting especially if we consider that \( \mu = 1.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1} \) is a mean value.

3.3. nc-Si:H TFTs
Results regarding the nc-Si:H TFTs can be seen in Fig. 4, where the transfer characteristics of two devices with different W/L ratios are shown. The mean parameters obtained in this case are also presented in Table 1.

Excellent subthreshold slope (0.34 V/dec) and mobility values (~11.5 cm²V⁻¹s⁻¹) were obtained. Such $\mu$ values highly improve the application field of nc-Si:H TFTs. As an example, the active matrix addressing of Organic Light Emitting Diodes (OLED) flat panel can use such high mobility TFTs, as it requires high mobility to produce enough current, high uniformity of the TFTs performance on large area, and a process using deposition conditions similar to that of a-Si:H. All these needs are fulfilled by the present HWCVD-deposited nc-Si:H TFTs.

3.4. Stability under gate bias stress

In order to study their stability, both a-Si:H and nc-Si:H TFTs were stressed under -10 V gate bias. Fig. 5 shows the variation of the threshold voltage under stress for both kinds of transistors. As expected, the $V_T$ shift was more pronounced in the case of a-Si:H devices ($\Delta V_T \sim 5$ V), pointing to stability problems most likely attributable to meta-stable defect creation in the material [7], what can be related to the high hydrogen ($C_H \sim 12\%$) content measured in a-Si:H films deposited in the same conditions as those implemented in the devices under study. Conversely, nc-Si:H TFTs showed superior stability against gate bias stress. The small $V_T$ shift observed in this case ($\Delta V_T \sim 0.5$ V), imputable to the disordered structure of nc-Si:H [8], is another argument to use these TFTs in the OLED addressing.

4. Conclusions

Amorphous and nanocrystalline silicon thin films deposited by Hot-Wire CVD at low substrate temperature (200°C) have been successfully implemented in coplanar top gate n-type TFTs. Layers were deposited onto SiO₂ coated glass and gate insulation was achieved by means of high quality RF sputtered SiO₂.

a-Si:H devices exhibited mobility values of 1.3 cm²V⁻¹s⁻¹, which are very high taking into account the amorphous nature of the material. nc-Si:H TFTs presented mobility values as high as 11.5 cm²V⁻¹s⁻¹ and resulted in low threshold voltage shift (~ 0.5 V), what made them suitable to be used in the OLED addressing.
Acknowledgements

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References

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Table 1 Mean parameters measured for a-Si:H and nc-Si:H TFTs.

Fig. 1 Cross-section of the n-type top gate coplanar TFTs.

Fig. 2 Raman spectra of a-Si:H and nc-Si:H layers deposited at the same conditions that those implemented in the TFTs.

Fig. 3 Transfer characteristics of a HWCVD a-Si:H TFT.

Fig. 4 Transfer characteristics of HWCVD-deposited nc-Si:H TFTs with different W/L ratios.

Fig. 5 Threshold voltage shift under –10 V gate bias for both a-Si:H and nc-Si:H TFTs.
### Table 1

<table>
<thead>
<tr>
<th></th>
<th>$\mu$ (cm$^2$V$^{-1}$s$^{-1}$)</th>
<th>$S$ (V/dec)</th>
<th>$V_T$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si:H</td>
<td>1.3</td>
<td>0.60</td>
<td>3.47</td>
</tr>
<tr>
<td>nc-Si:H</td>
<td>11.5</td>
<td>0.34</td>
<td>5.70</td>
</tr>
</tbody>
</table>
Figure 1

Glass substrate

- Al
- SiO₂
- n⁺ nc-Si:H
- Undoped a-Si:H or nc-Si:H
Figure 2
Figure 3

HWCVD a-Si:H

-5 0 5 10 15

10^-5

10^-6

10^-7

10^-8

10^-9

10^-10

10^-11

10^-12

-5 0 5 10 15

V_GS (V)

V_{DS} = 1V

Top Gate SiO_2 sputtering
W / L = 100 \mu m / 20 \mu m
Figure 4

HWCVD nc-Si:H

Top Gate: SiO₂ sputtering

- W / L = 80 μm / 60 μm
- W / L = 80 μm / 40 μm

VDS = 1 V
Figure 5

![Measurement Diagram]

- **HWCVD Top Gate TFT**
- **Sputtered SiO$_2$**
  - $\square$ a-Si:H
  - $\bullet$ nc-Si:H

**Measure:** $V_{ds} = 0.1V$

**Stress:** $V_{gs} = -10V$, $V_{ds} = 0V$, $T = 25^\circ C$