Thin-Film Transistors Obtained by Hot Wire CVD J. Puigdollers¹(1), A. Orpella(1), D. Dosev(2), C. Voz(3), D. Peiró(3), J. Pallarés(2), L.F. Marsal(2), J. Bertomeu(3), J. Andreu(3) and R. Alcubilla(1)

 Departament d'Enginyeria Electrònica. Jordi Girona 1-3, Mòdul C4. Universitat Politècnica de Catalunya (Barcelona, Spain).

(2) Departament d'Enginyeria Electrònica. Universitat Rovira i Virgili (Tarragona, Spain).

(3) Departament de Física Aplicada i Òptica. Universitat de Barcelona (Barcelona, Spain)

Abstract

Hydrogenated microcrystalline silicon films obtained at low temperature (150°C-280°C) by hot-wire chemical vapour deposition at two different process pressures were measured by Raman spectroscopy, X-ray diffraction spectroscopy and photothermal deflection spectroscopy. A high crystalline fraction (> 90%) with a low subgap optical absortion (10 cm⁻¹ at 0.8 eV) were obtained in films deposited at high growth rates (>0.8 nm/s). These films were incorporated in nchannel thin film transistors and their electrical properties were measured. The saturation mobility found was $0.72 \pm 0.05 \text{ cm}^2/\text{V}\cdot\text{s}$ and the threshold voltage around 0.2 eV. The dependence of their conductance activation energies on gate voltages were related to the properties of the material.

1. Introduction

Polysilicon thin-film transistors (TFTs) have become important as active elements in largematrix liquid crystal display (AMLCD)[1] applications such as portable devices and projection television [2]. For these applications TFTs have to be manufactured on a glass substrate; different approaches are being investigated with the aim of obtaining polycrystalline (poly Si) material at low temperatures (< 300°C). Some methods (such as solid phase crystallisation [3] and laser melting [4]) consist of the crystallization of amorphous silicon films obtained by different techniques (sputtering, plasma-enhanced chemical vapour deposition (PECVD)[5] or

¹Corresponding author

low-pressure chemical vapour deposition (LPCVD)[6]), while other approaches directly obtain polysilicon films.

Among the different deposition techniques for obtaining polysilicon films directly, hot-wire chemical vapour deposition (HWCVD) has drawn attention because of its effectiveness in obtaining device-quality hydrogenated microcrystalline silicon (μ c-Si:H) at low temperature (< 300°C) over large areas and at deposition rates (1 nm/s) [7,8,9]. The process pressure affects the structural properties of μ c-Si:H films obtained by HWCVD. Samples deposited at larger pressures (> 10⁻² mbar) have larger crystallite sizes and a smaller amorphous fractions than those obtained at smaller pressures (< 10⁻² mbar).

In this paper we report the application in TFTs of μ c-Si:H films deposited by HWCVD at different process pressures in the low substrate temperature range (< 280 °C). The structure of μ c-Si:H films deposited with different deposition parameters was determined by X-ray diffraction and Raman spectrometry. They were also electrically characterised by dark conductivity measurements. A series of n-channel TFTs were also made using the same deposition parameters. The resulting electrical properties were compared to material properties of the μ c-Si:H films.

2. Experimental

The hydrogenated microcrystalline silicon-thin films (μ c-Si:H) studied in this work were obtained by the hot-wire chemical vapour deposition (HWCVD) technique. The experimental set-up consists of two separate ultra-high vacuum chambers (for the doped and intrinsic material, respectively) with a load-lock chamber. The gas dissociation was achieved by means of a tungsten filament (0.5 mm diameter) which was heated to a temperature over 1700 °C. The μ c-Si:H films were deposited from a silane-hydrogen mixture at different process pressures and substrate temperatures (see Table 1). The μ c-Si:H films were simultaneously deposited on

Corning 7059 glass and on silicon dioxide (SiO₂) thermally grown on c-Si. Electrical properties of the films were obtained from coplanar conductivity measurements. The microstructure of the μ c-Si:H films was studied by Raman spectroscopy and X-Ray diffraction (XRD). Hydrogen content was determined from Fourier transform infrared spectroscopy. Finally, the optical absorption coefficient was measured by photothermal deflection spectroscopy (PDS).

	Pressure (10 ⁻² mbar)	T (°C)	SiH ₄ /H ₂ (sccm)	Deposition rate (nm/s)
HP	3.8 ± 0.1	150	4 / 76	0.8 ± 0.1
LP	0.7 ± 0.1	280	4/ 76	0.2 ± 0.1

Table1. Experimental deposition parameters.

Two series of thin-film Transistors (TFT) were made with the same technological deposition parameters as those used for high pressure (HP) and low pressure (LP) layers (see Table 1). We labelled TFT devices including μ c-Si:H deposited at high pressure and a substrate temperature of 150°C HP, and TFT devices including μ c-Si:H deposited at low pressure and a substrate temperature of 280°C LP.

A thermally oxidized n-type (100) silicon wafer with a resistivity of ~5 Ω -cm was used as a substrate. The TFTs are of the inverted-staggered structure with an intrinsic layer of 250 nm. The gate insulator was 250 nm thick. The HP TFTs devices had an n⁺ layer (50 nm) between the drain and source contact and the intrinsic layer. This n⁺ layer was also deposited by HWCVD with the same technological parameters as the HP intrinsic film but with 2 sccm of PH₃ added. The drain and source Cr contacts were thermally evaporated. All the devices had the same geometry: a channel width (W) of 137 µm and a length (L) of 55 µm. The electrical properties of the TFTs were measured under dark conditions by using a semiconductor parameter analyser (Hewlett Packard 4145B) and a programmable temperature controller (MMR Technologies K–20).

3. Results

Figure 1 shows the Raman spectra of the μ c-Si:H films deposited on Corning glass in the two deposition regimes. Both spectra have crystalline components with a crystalline fraction (X_C) obtained by deconvoluting the amorphous (480 cm⁻¹) and crystalline (520 cm⁻¹) contributions of 84% for the sample obtained at the smallest pressure (LP) and 93 % for the sample obtained at the other pressure (HP).

X-ray diffraction measurements also showed differences in the cristallinity of the films deposited at different process pressures [10]. Films deposited at the smaller pressure had a (111) orientation although the (220) was also observed. On increase of the process pressure, the films became gradually more oriented along the (220) direction. For the sample deposited at a pressure of $3.8 \cdot 10^{-2}$ mbar directions other than the (220) were not detected.

The hydrogen content, obtained by integrating the Si-H wagging band of the FTIR spectra [11], was around 3.5% and no variation, within errors of measurement, with the process pressure was observed. The electrical properties of these layers were $\sigma_{dark}=3.7\pm0.1 \times 10^{-6} \Omega^{-1} \text{cm}^{-1}$ and $E_{act}=0.56 \pm 0.02 \text{ eV}$ for the HP layer, and $\sigma_{dark}=1.3\pm0.1 \times 10^{-6} \Omega^{-1} \text{cm}^{-1}$ and $E_{act}=0.45 \pm 0.02 \text{ eV}$ for the HP layer, and $\sigma_{dark}=1.3\pm0.1 \times 10^{-6} \Omega^{-1} \text{cm}^{-1}$ and $E_{act}=0.45 \pm 0.02 \text{ eV}$ for the LP layer. Actually, a problem often encountered with as-grown undoped microcrystalline silicon is that it is generally n-type [12]. It was suggested that either the content of oxygen impurities or native defects within the layers could be responsible for this unwanted Fermi level shift [13].

Figure 2 shows the PDS absorption spectra for the samples obtained at LP and HP process pressure. This measurement was performed on 1 μ m thick samples deposited onto Corning glass. For comparison, the spectrum of an a-Si:H film deposited by RF glow discharge and the spectrum of monocrystalline silicon are also shown in the same Figure. Assuming that the optical absorption of μ c-Si:H can be considered as the contribution of the corresponding amorphous and crystalline phases, the spectra indicate that the HP is more crystalline than the LP sample. For example, for photon energies less than 1.7 eV the optical absorption coefficient of the LP sample is smaller than the monocrystalline silicon absorption, whereas for higher photon energies it is closer to the amorphous spectrum. This result confirms the different crystalline fractions deduced from Raman spectroscopy for both samples. Even though the HP sample had a crystalline fraction >90%, its optical absorption at photon energies >1.5 eV was greater than that of monocrystalline silicon. This effect we attributed to light scattering due to surface roughness rather than to an amorphous phase absorption. Finally, the subgap absorption, which is related to transitions between the bands and states located in the bandgap, is similar to device-quality amorphous silicon, which we suggest is due to a small density of states. In addition, the affect of light scattering could give an apparently larger subgap absorption, which could be related to a better hydrogen passivation of these films.

Figure 3 shows the output of drain-source current (I_{DS}) vs drain-source voltage (V_{DS}), for different gate-source voltages (V_{GS}) for the HP TFT device. The output has saturation levels acceptable in a device and no *kink* effect [14] was observed for larger V_{DS} . The output of the LP TFT device for smaller V_{DS} , where a small current crowding can be observed, is also shown (Figure inset). This effect indicates an affect of the contact resistance of the drain and source contacts, which is reasonable since this device had no doped layers. For the HP TFT device, which has an n⁺ layer between the electrodes and the μ c-Si:H layer, the smaller value of the contact resistance avoided the crowding effect.

The field-effect mobility (μ_S) and the threshold voltage (V_T) were determined from the I(V) in the saturation regime ($V_{GS}=V_{DS}$). By plotting the square root of $I_{DS}(V_{GS})$ in the saturation regime we deduced a mobility of 0.69 \pm 0.05 cm²·V⁻¹·s⁻¹ and a threshold voltage of approximately 0.3 V for the LP TFT. Similar results were obtained for the HP TFT device, with a higher mobility value 0.72 \pm 0.05 cm²·V⁻¹·s⁻¹ and a threshold voltage of ~0.2 V. The field-effect mobilities of both devices were thermally activated with an activation energy of about 0.1 eV.

Figure 4 shows the transfer properties obtained at different temperatures with a fixed drainsource voltage of 10 V for the LP TFT device. An exponential increase of I_{DS} with V_{GS} is observed for smaller V_{GS} , followed by a linear increase in current at other voltages. Drain currents of 1 μ A can be obtained for gate voltages <10 V. From the results shown in Figure 4 we obtain the conductance of the channel ($G_{DS}=I_{DS}L/V_{DS}W$) and its temperature dependence as a function of the gate voltage. Therefore the activation energy (E_{act}) of the conductance can be plotted as a function of the gate bias.

Figure 5 shows the variation of E_{act} ($E_{act}=E_C-E_F$) on gate bias obtained for the HP TFT and LP TFT devices. The E_{act} (and therefore the E_F position) depends on the gate voltage applied due to the band bending which takes place at the interface μ c-Si:H / SiO₂ upon application of an electric field perpendicular to the layers of the device.

4. Discussion

The application of a gate voltage in field effect structures shifts the Fermi level (E_F) inside the energy gap. With this displacement the electronic transport properties of the μ c-Si:H material can be measured [15]. The rate at which E_F moves towards the conduction band (in an n-channel device) depends on the density of electronic states located in the band gap and on the distribution of tail states close to the conduction band [16].

The sheet conductance activation energy of the LP TFT saturates at around 0.15 eV, whereas it saturates at around 0.1 eV in the HP device. Since the minimum of E_{act} could be taken as a measurement of the width of the distribution of conduction band tail states [17], we can infer that the band tail density of states of the material used to manufacture LP TFT are greater than those used to manufacture HP TFT. This increase could be related to an increase of the amorphous phase, in agreement with Raman measurements (Figure 1).

The activation energies at $V_{GS}=0$ were 0.26 ± 0.02 eV and 0.37 ± 0.02 eV for the LP and HP TFT devices, respectively. These energies are less (about 0.2 eV in both cases) than those

obtained when μ c-Si:H layers (thicker than 1 μ m and deposited on Corning glass) deposited with the same technological parameters as the devices whose electrical properties were measured [section §3].

When a negative V_{GS} is applied, a hole accumulation is formed near the SiO₂ / μ c-Si:H interface and the rest of the layer becomes slightly n-type. Therefore, two conduction paths can be considered: a p-type channel near the interface and the rest of the μ c-Si:H layer which is moderately n-type.

The variation of the activation energy for negative V_{GS} shows differences between both devices due to the absence of the n⁺ layer in the LP TFT device. Without a doped layer, neither the electrons nor the holes are blocked by the ohmic chromium contacts. Therefore, both conduction paths can contribute to the measured I_{DS} current and the measured activation energy corresponds to the less resistive path. When larger negative V_{GS} are applied, the main contribution to the conduction is determined by the p-type path near the SiO₂ / μ c-Si:H interface. The measured activation energy corresponds to this part of the channel and decreases when the applied V_{GS} increase the hole concentration within this conduction path.

When an n^+ doped layer is included, as in the HP TFT device, the p-type path is blocked and the measured activation energy corresponds to the moderately n-type remainder of the channel. Consequently, the activation energy does not reach midgap and decreases when higher larger V_{GS} are applied.

5. Conclusions

Device quality μ c-Si:H was obtained with fast growth rates (0.8 nm/s) and low substrate temperatures (150 °C) by the HW-CVD technique. Undoped μ c-Si:H, incorporated in field-effect thin-film transistors, had acceptable properties and saturation levels for a device. A field-effect mobility of 0.7 cm²/Vs and threshold voltages <0.3 eV are similar to the best reported mobilities and voltages for similar μ c-Si:H devices obtained by HW-CVD.

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Figure captions.

Figure 1. Raman spectra for µc-Si:H deposited on glass substrate at high pressure (HP) and low pressure (LP).

Figure 2. Optical absorption spectra of HP and LP layers measured by PDS. The spectra of a hydrogenated amorphous silicon (a-Si:H) film and of monocrystalline silicon (c-Si) are also shown.

Figure 3. Transistor output characteristics for HP TFT. In the inset the output characteristics for low V_{DS} of LP TFT are shown (lines are drawn as guide to the eye). Gate-source voltage varied between 12 V and 40 V at intervals of 4 V for both devices.

Figure 4. Temperature dependence of the transfer characteristics of the LP TFT (lines are drawn as guide to the eye).

Figure 5. Comparison of the drain-source conductance activation energy for LP TFT (without nlayer) and HP TFT (with n-layer). Lines are drawn as guide to the eye.



Figure 1.



Figure 2.



Figure 3.



Figure 4.



Figure 5.