Improvement of the Quality Factor of RF Integrated Inductors by Layout Optimization

José M. López-Villegas, *Member, IEEE*, Josep Samitier, *Member, IEEE*, Charles Cané, Pere Losantos, and Joan Bausells, *Member, IEEE*

***Abstract*—A systematic method to improve the quality (Q) factor of RF integrated inductors is presented in this paper. The proposed method is based on the layout optimization to minimize the series resistance of the inductor coil, taking into account both ohmic losses, due to conduction currents, and magnetically induced losses, due to Eddy currents. The technique is particularly useful when applied to inductors in which the fabrication process includes integration substrate removal. However, it is also applicable to inductors on low-loss substrates. The method optimizes the width of the metal strip for each turn of the inductor coil, leading to a variable strip-width layout. The optimization procedure has been successfully applied to the design of square spiral inductors in a silicon-based multichip-module technology, complemented with silicon micromachining postprocessing. The obtained experimental results corroborate the validity of the proposed method. A Q factor of about 17 have been obtained for a 35-nH inductor at 1.5 GHz, with Q values higher than 40 predicted for a 20-nH inductor working at 3.5 GHz. The latter is up to a 60% better than the best results for a single strip-width inductor working at the same frequency.**

***Index Terms*—Inductor layout optimization, integrated RF inductor, silicon micromachining for RF applications, silicon RFIC's.**

I. Introduction

ONE OF THE key factors that determines the performance of RF integrated circuits (RFIC's) is the availability of good quality integrated inductors. Unfortunately, parasitic effects, such as coupling capacitance and losses related to the integration substrate, affect these components, degrading their performance. These unwanted effects are particularly important using silicon substrates [1], [2].

Recently, the use of silicon micromachining techniques to remove the integration substrate underneath the planar inductors has significantly increased both the inductor self-resonant frequency and quality (Q) factor [3]–[6]. Silicon micromachining techniques have also been used to provide individual shielding and self-packaging of transmission lines and other RF components and circuits [7], [8]. As a consequence of all this, the concept of RF micromachining is becoming more widely utilized in the field of RFIC design.

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Once the silicon substrate is removed, other factors that also degrade the inductors performance become relevant and must be taken into account. Among them, magnetically induced currents on the inductor coil (Eddy currents) [9] could be the most significant. These currents are directly dependent on the time varying magnetic flux through the metal strip used to fabricate the inductor spiral. The direct consequences of these currents are frequency dependent losses, which increase as the metal strip width increases.

In the usual case of a spiral inductor fabricated using a constant width metal strip, the influence of magnetically induced losses is much more important in the inner turns of the coil, where the magnetic field reaches its maximum. According to this, some authors proposed the elimination of the central turns to reduce losses [9]. However, this is not the best procedure to improve the inductor Q factor.

The objective of this paper is to find a systematic method to optimize the integrated inductor layout in order to reach maximum the Q factor, with the analysis of the inductor coil series resistance. Both ohmic losses, related to conduction currents, and magnetically induced losses, related to Eddy currents, are taken into account in our analysis. Section II is devoted to illustrate the influence of these losses on the inductor's performance by comparing experimental measurements and numerical simulation using an electromagnetic planar solver. In Section III, the layout optimization method is presented. Section IV is devoted to illustrate the application of the method to the design of square spiral inductors in a silicon based multichip-module (MCM-D) technology complemented with silicon micromachining post processing. This section also shows the obtained experimental results, which corroborate the validity of the proposed method. Finally, Section V summarizes the conclusions.

II. Inductor's Losses Analysis

The overall integrated inductor losses can be divided into two main contributions [6]: integration substrate losses and strip metal losses, both of which are discussed in detail in this section.

A. Substrate Losses

Due to the relatively low resistivity of silicon (in comparison with GaAs), substrate losses are the most important factor degrading the performance of silicon integrated RF inductors. A major source of substrate losses is the capacitive coupling that allows conduction current flow not only through the metal strip, but also through the silicon substrate. Another important source

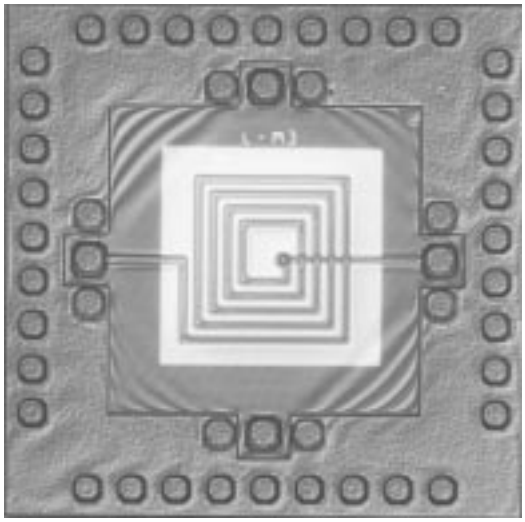

Fig. 1. . Top-view photograph of a four-and-one-half-turn square spiral RF integrated inductor, performed using silicon-based MCM technology, complemented with silicon micromachining postprocessing. The light square in the center corresponds to the area where silicon has been removed.

of substrate loss is the inductive coupling. Due to the planar geometry of the inductor, the magnetic field penetrates deep into the silicon substrate, inducing currents loops and related losses. These effects are particularly important for large-area inductors. Fortunately, the development of silicon micromachining techniques, compatibles with standard silicon technologies, has overcome this problem.

To illustrate this point, consider the electrical behavior of the inductor shown in Fig. 1. The inductor structure is a four-and-one-half-turn square spiral formed using thee metal levels MCM-D silicon-based technology. The inductor coil is performed using the top metal level ($M3$), with sheet resistance of 20 mΩ. The metal strip of the coil is 30-μm wide and the turn-to-turn spacing is 20 μm. At the center of spiral, a via connects the $M3$ level with the next metal level $M2$ (same sheet resistance as $M3$), then a 30-μm-wide metal strip crosses underneath the coil to allow external access. Two RF pads, ground–signal–ground (GSG) are located on the left- and right-hand sides, which are connected to the outer turn of the coil and to the crossing strip, respectively. Top and bottom RF pads are not connected in this case. A ground ring constructed by interconnecting $M1$, $M2$, and $M3$ metal levels surrounds the inductor structure. Finally, etching windows are defined on the backside of the wafer to remove the silicon substrate underneath the inductor coil. The photograph shown in Fig. 1 has been obtained using both front and back illumination, which allow us to see the area where silicon has been removed as a lighter square.

Fig. 2 schematically depicts the cross section of the integration substrate underneath the inductor. It is composed of three p-type silicon layers, in which thickness and resistivities are: 375 μm, 0.01 Ωcm; 16 μm, 10 Ωcm and 4 μm, 1 Ωcm; respectively. Over them are a silicon dioxide layer 3- μm thick and three polyimide layers 4-μm thick. $M1$ metal level lays on the silicon dioxide layer, while $M2$ and $M3$ metal levels are located between the polyimide layers.

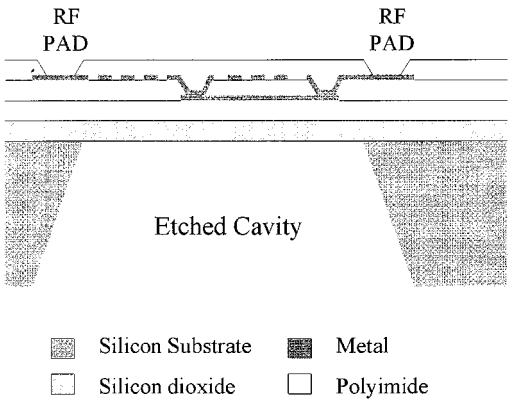

Fig. 2. Cross view of the integration substrate underneath the inductor structure after silicon removal.

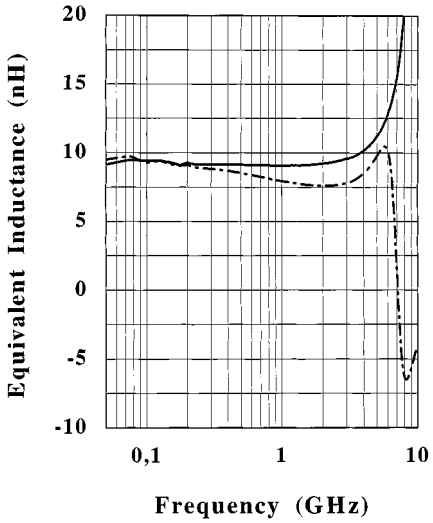

Fig. 3. Equivalent inductance of the structure shown in Fig. 1. Dot–dashed line corresponds to data before silicon removal. Continuous line corresponds to data after etching of the silicon substrate.

The scattering parameters of the inductor have been measured in the range from 50 MHz to 10 GHz using an HP8720C Vector Network Analyzer. The on-wafer measurements have been made using a couple of ACP-40 GSG air coplanar microprobes from Cascade Microtech Inc., Beaverton, OR. In order to set the measurement reference planes at the probe tips, a line–reflect–match (LRM) calibration procedure has been used. The standards required for the calibration process are included in an LRM ISS 101 190 (GSG) impedance standard substrate, also from Cascade Microtech Inc.

Fig. 3 shows the inductor equivalent inductance and Fig. 4 the inductor Q factor, both extracted from the measurements of the scattering parameters. Data obtained before and after silicon substrate removal are compared in these figures. As we can see, removing the substrate leads to an increase in the self resonant frequency (evaluated as the frequency at which the equivalent inductance cross zero) and in the maximum Q factor of the inductor. The former parameter changes from about 7 GHz, before silicon removal, to more than 10 GHz after etching. Much more important is the increase in the Q factor. Its maximum value changes from 3.5 (at 1.25 GHz) to about 20 (at 5 GHz), before and after etching, respectively.

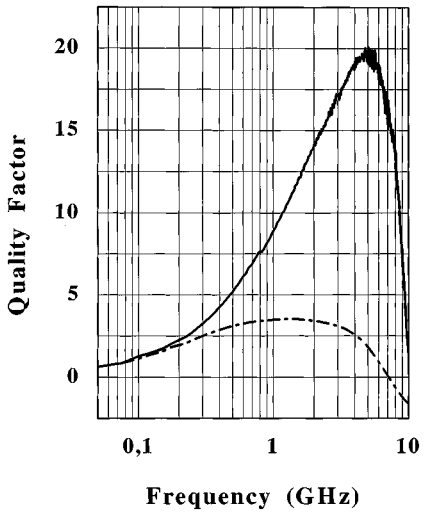

Fig. 4. Q factor of the inductor structure shown in Fig. 1. Data before silicon removal: (– - –) . Data after etching of the silicon substrate: (—).

B. Metal Losses

Once the substrate is removed, losses are mainly related to the metal strip resistance. An accurate analysis of this parameter requires taking into account conduction losses and magnetically induced losses. One way to evaluate the influence of each of these contributions on the overall metal losses is by means of electromagnetic simulation tools, used to reproduce the inductor electrical behavior under different conditions. In our case, HP momentum planar solver has been used to simulate the S-parameters of the inductor, shown in Fig. 1. To reproduce as close as possible the actual inductor, the simulation substrate includes the complete set of layers of the available MCM-D technology. Substrate removal is reproduced in the simulations using air layers instead of silicon layers in the substrate definition process.

In a first set of simulations, the inductor coil has been meshed in simple cells, as shown in Fig. 5(a). In each cell, an average current density vector is defined. Consequently, the influence of induced current loops, like Eddy currents, are not taking into account in the simulation results because their average value on each cell is zero. Therefore, the simulation process can only reproduce losses related to the sheet resistance of the metal strip.

If we want to take into account the influence of induced current loops, a more accurate mesh has to be done. Fig. 5(b) shows the refined mesh used in our second set of simulations. As we can see, each previous cell is divided into three new ones, allowing current redistribution in the metal strip. In both sets of simulations, the sheet resistance of the metal strip is frequency dependent to take into account skin effect. Figs. 6–8 show the obtained simulation results in comparison with the experimental data.

Let us first consider the results before etching. Fig. 6 shows the inductor equivalent inductance and Fig. 7 the inductor Q factor. The electromagnetic simulator using either the simple or refined mesh reproduces very well the experimental equivalent inductance. Only small differences are observed between meshing procedures on the inductor Q factor. That is, the influence of the silicon substrate, which is the most important loss

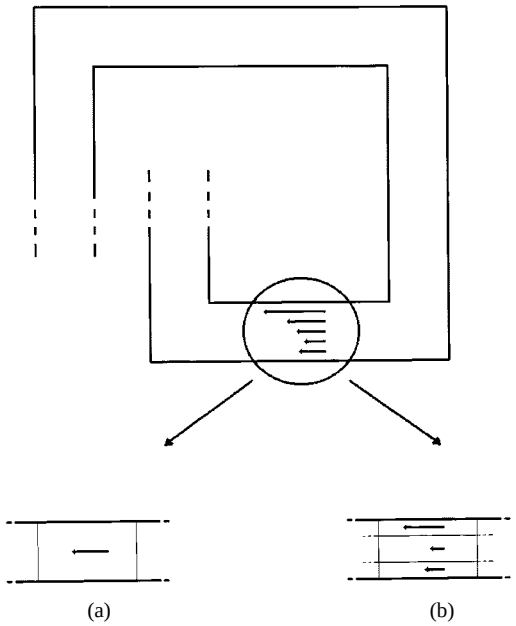

Fig. 5. Qualitative graph showing the two meshing procedures used to simulate the inductor's electrical behavior. (a) Simple mesh. (b) Edge mesh.

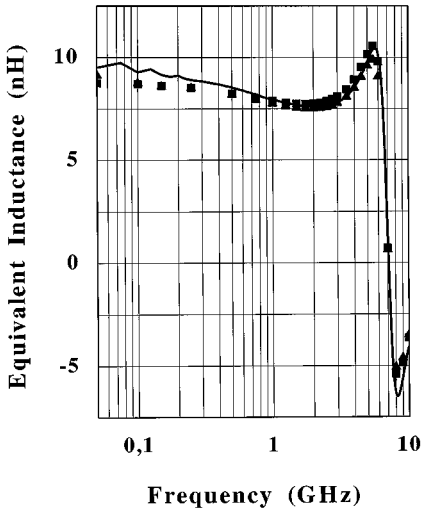

Fig. 6. Comparison of the experimental and simulated equivalent inductance before silicon removal. The continuous line corresponds to the experimental data, ■ are the simulated results obtained using simple mesh, and ▲ are the simulated results obtained using edge mesh.

factor, is properly taken into account in both simulations. Thus, in this case, the improvement in the simulation accuracy due to the use of refined mesh does not justify the increase in the requirements of memory and computation time.

After substrate removal, the equivalent inductance is also very well reproduced using either simple or refined meshing procedures. However, strong differences are observed in the inductor Q factor, as shown in Fig. 8. Simple meshing always predicts Q factors higher than experimental values for any frequency in the operating range. On the contrary, using the refined meshing procedure, the simulator reproduces quite well the experimental Q factor. Only few differences are observed, which could be reduced using a finer mesh, but at the expense of an increase in memory and computation time.

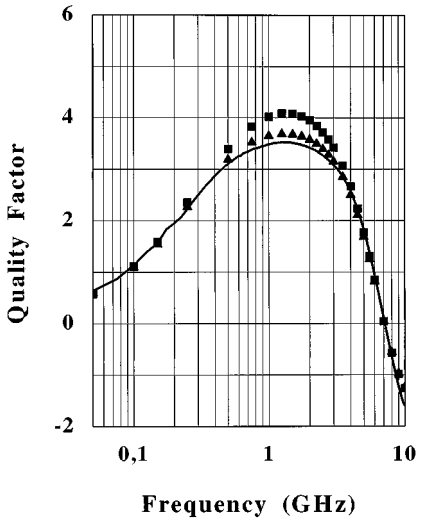

Fig. 7. Comparison of the experimental and simulated Q factor before silicon removal. Continuous line corresponds to the experimental data, ■ are the simulated results obtained using simple mesh, and ▲ are the simulated results obtained using edge mesh.

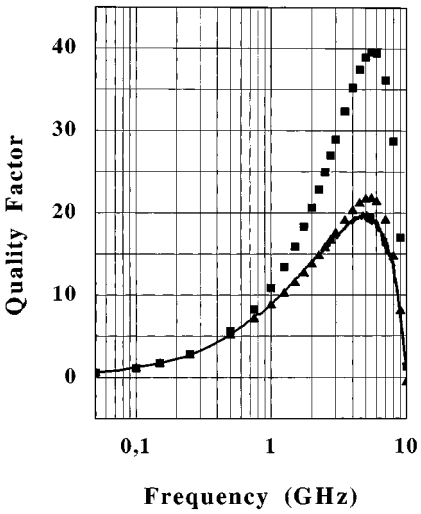

Fig. 8. Comparison of the experimental and simulated Q factor after silicon removal. Continuous line corresponds to the experimental data, ■ are the simulated results obtained using simple mesh, and ▲ are the simulated results obtained using edge mesh.

We conclude that the electromagnetic planar solvers are a powerful tool in the design of RF integrated inductors, provided the adequate simulation conditions are used. In Section III, we will use an HP Momentum planar solver to develop the inductor layout optimization method in the case of micromachined integrated inductors.

III. Description of the Layout Optimization Method

The starting point of the proposed method is the study of the series resistance of the inductor coil. This parameter has two main contributions. First, the contribution related to the sheet resistance of the metal strip, which is inversely proportional to the metal strip width. Second, the contribution related to magnetically induced losses, which directly depend on the time derivative of the magnetic-field flux through the metal strip. Consequently, in the later case, a contribution to the coil resistance that increases with both frequency and metal strip width is expected. Thus, an optimum strip width, which minimizes series resistance and maximizes the Q factor will occur, as shown in Fig. 9. The Q factors of different 20-nH inductors are plotted as a function of the metal strip width for several values of the operating frequency. All the inductors are simulated using the previous MCM-D set of layers. The inductor layout is an eight-turn square spiral and the turn-to-turn spacing s and the metal strip width w satisfies the condition $w + s = 50\ \mu$m.

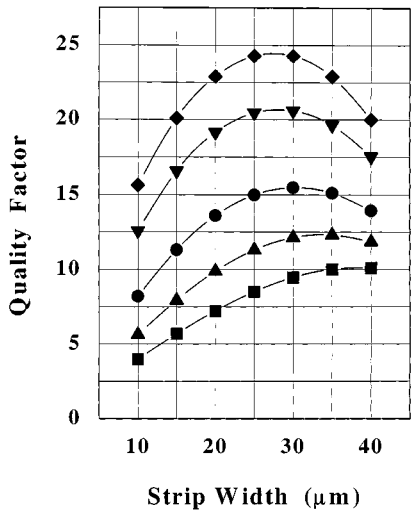

Fig. 9. Q factor as a function of the metal strip width for different 20-nH RF integrated inductors. ■ are the obtained Q factors at 0.7-GHz frequency of operation, ▲ 1 GHz, • 1.5 GHz, ▼ 2.5 GHz, and ♦ 3.5 GHz.

As is clearly shown from Fig. 9, the strip width that optimizes the inductor Q factor for a given frequency is easily obtained by doing a small number of simulations. Although this procedure can be used to optimize the inductor Q factor, better results can be obtained if a different strip width is used for each turn of the coil. Narrow strips optimize losses in the inner turns, where magnetic field reach its maximum, while wide strips optimize the outer turns, where ohmic losses are predominant. Consequently, we have to evaluate the magnetic-field distribution across the inductor structure to obtain the best set of strip-width values. Thus, let us assume that for any turn of the coil, the strip width is smaller than the turn length. Moreover, the whole coil length is smaller that the wavelength at the operating frequency. Under these assumptions, each turn of the coil can be considered as a square current loop. Furthermore, there are not significant phase differences between currents at any place in the coil. In this case, the magnetic field in the nth turn of the coil can be approximated by

$$B_n = B_{n,n} + B_{n,\mathrm{in}} + B_{n,\mathrm{out}} \tag{1}$$

where: 1) $B_{n,n}$ is the magnetic field at turn n generated by itself; 2) $B_{n,\mathrm{in}}$ is the magnetic field at turn n generated by the inner turns (taking turn n as a reference position); and 3) $B_{n,\mathrm{out}}$ is the magnetic field at turn n generated by the outer turn. These fields have been calculated by averaging the values in the middle

of one side of the nth turn and in one vertex, giving the following expressions:

$$B_{n,n} = \frac{\mu_o I}{4\pi\, d_n}\left(\frac{\sqrt{5}}{2} + \frac{\sqrt{2}}{4}\right) \tag{2a}$$

$$B_{n,\text{in}} = \frac{\mu_o I}{4\pi}\sum_{k=1}^{n-1}\left(-\frac{\sqrt{d_k^2+(d_n-d_k)^2}}{d_k(d_n-d_k)} + \frac{\sqrt{d_k^2+(d_n+d_k)^2}}{d_k(d_n+d_k)} + \sqrt{2}\frac{d_n}{d_n^2-d_k^2} - \frac{\sqrt{(d_n-d_k)^2+(d_n+d_k)^2}}{d_n^2-d_k^2}\right) \tag{2b}$$

$$B_{n,\text{out}} = \frac{\mu_o I}{4\pi}\sum_{k=n+1}^{N}\left(\frac{\sqrt{d_k^2+(d_k-d_n)^2}}{d_k(d_k-d_n)} + \frac{\sqrt{d_k^2+(d_k+d_n)^2}}{d_k(d_k+d_n)} + \sqrt{2}\frac{d_k}{d_k^2-d_n^2} + \frac{\sqrt{(d_k-d_n)^2+(d_k+d_n)^2}}{d_k^2-d_n^2}\right). \tag{2c}$$

In these expressions, μ_o is the magnetic permeability of vacuum, I is the current passing through the metal strip, N is the number of turns, and d_n is given by

$$d_n = \frac{l_n}{8} \tag{3}$$

where l_n is the length of the nth turn of the coil, which, in the case of a square spiral, can be expressed as

$$l_n = l_{n-1} + s_{n-1} + 6s_n + s_{n+1} + \frac{7w_{n-1}+9w_n}{2} \tag{4}$$

with w_n the width of the nth turn of the coil and s_n the spacing between turns n and $(n-1)$.

According to (2), the magnetic field B_n can be expressed as follows:

$$B_n = g_n I \tag{5}$$

where g_n is a function dependent only on geometrical parameters such as: 1) N, which is the number of turns; 2) l_1, which is the length of the first turn of the coil; 3) w_n, which is the metal strip width; and 4) s_n, which is the turn-to-turn spacing (from $n=1$ to N). Inductor geometry other than square spirals (i.e., octagonal inductors) can easily be considered using the correct expression for the g_n function. That is, rewriting (2)–(4) for the new geometry.

The simple model used to describe the magnetic field will fail as the desired optimum frequency increases, and the wavelength approaches the total length of the coil. This problem could be partially avoided by introducing in (2) corrective factors to take into account the phase shift between currents flowing in the different turns of the coil.

Once the magnetic field is known, using Faraday's law, we can obtain the induced electric field E_n for each turn of the coil using

$$\oint E_n\, dc = -\frac{d\Phi_n}{dt} \tag{6}$$

where dc is the contour element and ϕ_n is the magnetic field flux through the metal strip at the nth turn. Taking into account the coil geometry, (6) becomes in a first approach

$$2\, l_n E_n = -w_n l_n \frac{dB_n}{dt}. \tag{7}$$

The induced field E_n has the direction of the current flow on one edge of the metal strip (usually the inner edge) and the opposite direction on the other. As a consequence of this induced field, redistribution occurs in the current flowing through the metal strip. In particular, the current density will increase near one of the metal edges and decrease near the other in the same amount, which is given by

$$\Delta j_n = \sigma E_n = -\frac{w_n}{2}\frac{dB_n}{dt}\sigma. \tag{8}$$

Although the average current passing through the metal strip does not change, losses will increase in a factor that is proportional to Δj^2. Taking this into account and assuming a sinusoidal dependence for the current passing through the metal strip, we can obtain the following expression for the series resistance of the coil R_s:

$$R_s = \sum_{n=1}^{N}\left[\frac{r_s(f)}{w_n} + C g_n^2 f^2 w_n^2\right] l_n \tag{9}$$

where $r_s(f)$ is the sheet resistance of the metal strip, f is the frequency, and C is a constant, which can be obtained by fitting the experimental or simulated results. For instance, in the case of a constant strip-width inductor, (9) has a minimum for a width w_{opt} given by

$$w_{\text{opt}} = \sqrt[3]{\frac{r_s(f)}{2kf^2}} \tag{10}$$

with

$$k = C\frac{\sum_{n=1}^{N} g_n^2 l_n}{\sum_{n=1}^{N} l_n}. \tag{11}$$

For a given inductor geometry and frequency of operation, by comparing the experimental or simulated optima widths (i.e., those in Fig. 9) with the predicted value of (10), we can obtain k. Then, using (11), we obtain C.

Finally, once the fitting parameter C is known, we can obtain the set of optima strip-width values by minimizing R_s as a

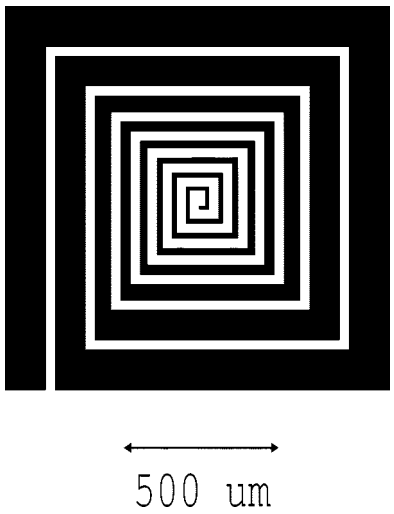

Fig. 10. Optimized 20-nH inductor's layout for a working frequency of 3.5 GHz.

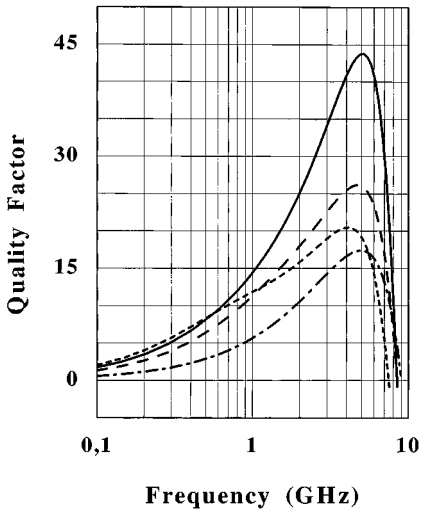

Fig. 11. Q factor as a function of frequency for different eight-turns 20-nH RF integrated inductors: (– - –) corresponds to an inductor performed using a metal strip 10-μm wide, (– – –) 25 μm, (- - - - - -) 40 μm, and (—) optimized layout of Fig. 10.

function of n variables w_n ($n = 1, \cdots, N$). Thus, for any turn of the coil, we find an optimum width $w_{\mathrm{opt},\,n}$ given by

$$w_{\mathrm{opt},\,n} = \sqrt[3]{\frac{r_s(f)}{2\,C g_n^2 f^2}}. \tag{12}$$

Therefore, we propose an iterative method to optimize the inductor layout in order to reach the maximum Q factor at a given frequency. The main steps are as follows.

1) An initial set of strip-width values is defined (i.e., the same strip-width value for all the turns).
2) Taking into account the strip-width values and other geometric parameters defining the inductor layout (i.e., number of turns N, turn-to-turn spacing $s_{n,}$, and length of the first turn of the coil l_1, l_n, and d_n are calculated for each turn using (3) and (4).
3) Using (1) and (2), the magnetic field is evaluated, and using (5), the values of g_n function are calculated.
4) Finally, the set of strip widths $w_n(n = 1, \cdots, N)$ is updated using (12).
5) The process stops here if the desired accuracy in the set of strip-width values is reached, if not, back to (2), and so on.

This procedure has been used to obtain the optimized layout shown in Fig. 10. The inductor geometry is an eight-turn square spiral, being the turn-to-turn spacing 30 μm. The optimum frequency of operation is 3.5 GHz. An HP Momentum simulator has been used to evaluate the performance of this optimized layout when implemented using the available MCM-D + silicon micromachining technology. The value of the equivalent inductance at the low-frequency plateau is found to be about 20 nH, and the self-resonant frequency is about 8 GHz. In Fig. 11, the inductor Q factor is plotted as a function of frequency. The same figure also presents the Q factors of some eight turn 20-nH inductors, with data shown in Fig. 9.

Quite good results are expected using the proposed method. At the frequency of operation, the optimized layout shows a Q factor of more than 40, which is about 1.6 times that of the best single strip-width inductor. Moreover, high Q factors are obtained over a wide range of frequencies around the optimum value of 3.5 GHz.

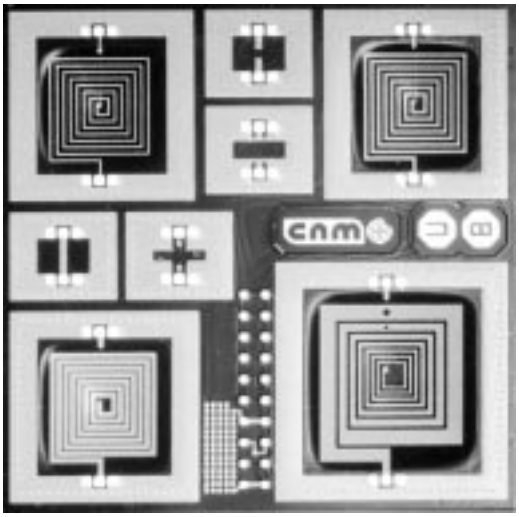

Fig. 12. Top-view photograph of the IC designed to test the inductor's layout optimization method. Three constant strip-width inductors are integrated together with the optimized layout. Some test structures are also included to allow pad deembedding purposes.

IV. Experimental Results

In order to confirm the validity of the proposed layout optimization method, a set of square spiral inductors has been designed and measured. Fig. 12 shows a photograph of the integrated circuit (IC), which has been performed using the available MCM-D + Si micromachining technology. Three constant width inductors of 16-μm wide (top left-hand side), 36-μm (top right-hand side), and 51-μm (bottom left-hand side) have been implemented together with the optimized layout (bottom right-hand side). The IC also includes some test structures for calibration purposes and pad deembedding.

For all the structures shown on Fig. 12 the equivalent inductance at the low frequency plateau is 34 ∓ 1 nH. In this case we

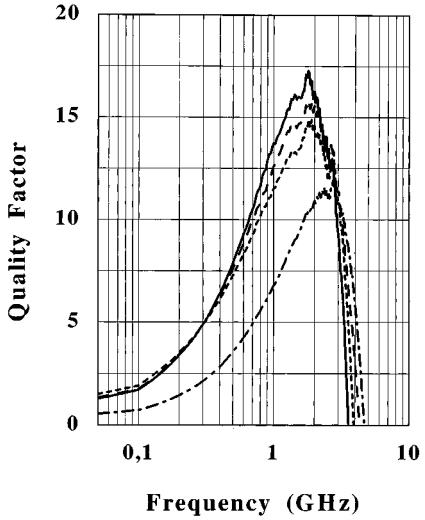

Fig. 13. Experimental Q factors as a function of frequency for the inductor structures on Fig. 12. (– - –) corresponds to the inductor performed using a metal strip 16-μm wide, (– – –) 36 μm, (- - - - - -) 51 μm, and (—) optimized layout.

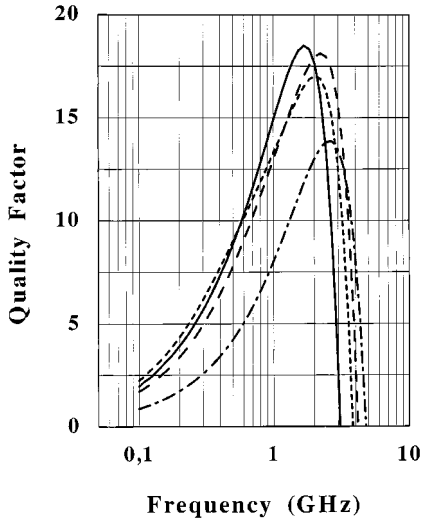

Fig. 14. Simulated Q factors as a function of frequency for the inductor structures on Fig. 12. (– - –) corresponds to the inductor performed using a metal strip 16-μm wide, (– – –) 36 μm, (- - - - - -) 51 μm, and (—) optimized layout.

were interested in optimizing the inductor layout for a working frequency of 1.5 GHz. The obtained Q factors versus frequency are plotted on Figs. 13 (experimental data) and 14 (Momentum simulations).

Good agreement is observed between measurements and simulations, which validates the proposed layout optimization method. The optimized layout shows the best performance of all the structures from about 600 MHz to 2 GHz. Q value of 17 at 1.5 GHz has been obtained for a 34-nH inductor, which, as far as we know, is one of the best reported results for an integrated inductor using silicon technologies. Finally, the improvement of the Q factor after optimization is not as important as in the previous design example because of the lower frequency of operation. In general, provided the total length of the inductor coil is small in comparison with the wavelength—the higher the working frequency the better the optimized layout performance will be. In practice, for inductance values from several nanohenrys to several tens of nanohenrys, the proposed method has been successfully applied to optimize the inductor layout for working frequencies in the range from 1 to 10 GHz.

V. Conclusion

This work is devoted to the study of RF integrated inductors performed as planar square spirals in a silicon-based MCM-D technology complemented with silicon micromachining techniques. The inductor series resistance is analyzed taking into account both ohmic losses, due to conduction currents, and magnetically induced losses, due to Eddy currents. Both contributions are accurately reproduced using electromagnetic planar solvers, provided the adequate simulation conditions are used.

From the analysis of the inductor series resistance, a systematic method to improve the Q factor of RF integrated inductors is presented. The method is based on the layout optimization being the width of the metal strip used to perform the inductors coil of the optimization variable. For a given frequency of operation, the application of the proposed method minimizes the series resistance of each turn of the inductor coil, leading to a multistrip-width layout. This procedure give the best results when applied to inductors in which the fabrication process includes the removal of the integration substrate underneath the inductor's coil. However, it can also be used to optimize the design of inductors laying on low-loss substrates.

Finally, the proposed method is used to optimize the layout of square spiral inductors. Nevertheless, the method can easily be adapted to optimize other inductor geometry (i.e., octagonal spirals). The comparison of the results obtained for the optimized layout with those of other nonoptimized inductors (having the same equivalent inductance and number of turns of the coil) reveals that the application of the proposed method leads to a significant increase in the inductor Q factor. Values of Q of about 17 have been obtained for a 34-nH inductor at 1.5 GHz, which, to our best knowledge, is one of the best reported results for an integrated inductor using silicon technologies. Moreover, Q factors higher than 40 are predicted for a 20-nH inductor working at 3.5 GHz, which is up to 60% better than the best result for a single strip-width nonoptimized inductor.

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