Thermal Modeling and Management in Ultrathin Chip Stack Technology

Stéphane Pinel, Antoine Marty, Josiane Tasselli, Jean-Pierre Bailbe, Eric Beyne, Rita Van Hoof, Santiago Marco, Joan Ramon Morante, Olivier Vendier, and Marc Huan

***Abstract*—This paper presents a thermal modeling for power management of a new three-dimensional (3-D) thinned dies stacking process. Besides the high concentration of power dissipating sources, which is the direct consequence of the very interesting integration efficiency increase, this new ultra-compact packaging technology can suffer of the poor thermal conductivity (about 700 times smaller than silicon one) of the benzocyclobutene (BCB) used as both adhesive and planarization layers in each level of the stack. Thermal simulation was conducted using three-dimensional (3-D) FEM tool to analyze the specific behaviors in such stacked structure and to optimize the design rules. This study first describes the heat transfer limitation through the vertical path by examining particularly the case of the high dissipating sources under small area. First results of characterization in transient regime by means of dedicated test device mounted in single level structure are presented. For the design optimization, the thermal draining capabilities of a copper grid or full copper plate embedded in the intermediate layer of stacked structure are evaluated as a function of the technological parameters and the physical properties. It is shown an interest for the transverse heat extraction under the buffer devices dissipating most the power and generally localized in the peripheral zone, and for the temperature uniformization, by heat spreading mechanism, in the localized regions where the attachment of the thin die is altered. Finally, all conclusions of this analysis are used for the quantitative projections of the thermal performance of a first demonstrator based on a three-levels stacking structure for space application.**

***Index Terms*—Benzocyclobutene, copper, FEM, MCM, thermal simulation, thermal transient, thin dies, 3-D integration.**

I. INTRODUCTION

RECENT development of advanced packaging technologies such as three-dimensional (3-D) stacking, multichip modules (MCMs) and 3-D stacks of MCMs provided an opportunity for significant reduction in system mass, volume and power consumption [1]–[5]. During the last 30 years, the thickness of packages have been divided by ten. The advancement of thinning, transport and attachment technology and the modification of existing planarization and interconnection techniques has led to the use of Ultra Thin Chip Stacking (UTCS) technology [6]. This new integration technique we have studied can be described as follow (Fig. 1): chips are thinned down to 10 μm [7] and then, using planarization techniques as used in semiconductor processing, the 3-D stack is realized on a silicon substrate by depositing layers of BenzoCycloButene (BCB) onto which a metallization pattern is formed. The thinned chips are placed on top of each dielectric layer and the vertical interconnection is achieved with metallized vias. The final stack has a thickness comparable to the standard silicon chips one.

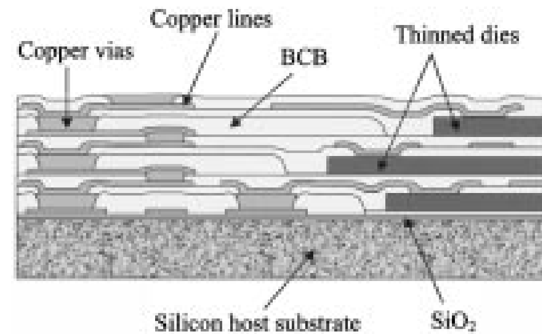

Fig. 1. Schematic of the ultra thin chip stacking technology configuration.

For this proposed technology, besides the imperatives dictated by the whole of the developed fabrication sequence and the induced residual thermomechanical stresses, characteristics of any heterogeneous assembly [8], the possible limitations by thermal dissipation effects can influence a lot on the design rules definition. Indeed, on the one hand, the vertical integration principle itself is an obvious factor of heat sources concentration, and on the other hand the use of BCB having a poor thermal conductivity, as adhesive and planarization layer, degrades the heat extraction efficiency through the vertical path.

This paper is precisely focused on the analysis of thermal behaviors for this novel compact integration technology by approaching the four following points:

1) the modeling of single-level structures and the study of a possible limitation by the low thermal conductivity of BCB layers;
2) a first characterization of a single level structure by the study of the transient thermal response;
3) a suggestion for the optimization of conductive thermal path in multilevel structures;
4) the thermal evaluation of our first demonstrator based on a three-levels stacking structure for space application.

Manuscript received January 30, 2001; revised January 23, 2002. This work was supported by the Esprit Project UTCS EP 24910. This work was recommended for publication by Associate Editor C. C. Lee upon evaluation of the reviewers' comments.

S. Pinel, A. Marty, J. Tasselli, and J.-P. Bailbe are with the Laboratoire d'Analyse et d'Architecture des Systèmes, CNRS, Toulouse Cedex 4 31077, France.

E. Beyne and R. Van Hoof are with IMEC, Leuven B-3001, Belgium.

S. Marco and J. R. Morante are with the Departament d'Electronica, Universitat de Barcelona, Barcelona 08028, Spain.

O. Vendier and M. Huan are with ALCATEL SPACE Industries, Toulouse Cedex 31037, France.

Publisher Item Identifier S 1521-3331(02)04733-5.

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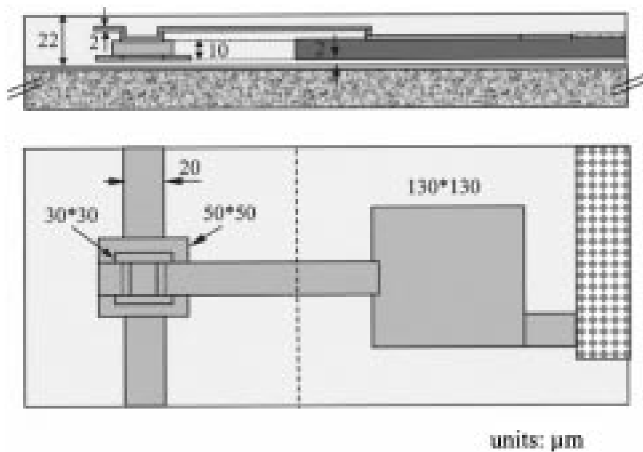

Fig. 2. Design rules of MCM-D technology considered in 3-D FEM thermal modeling.

This modeling approach, which one wishes as rigorous as possible, is based on 3-D FEM calculations. Analytical 1-D projections will come to support the analysis when that can be justified.

II. Modeling of Single-Level Structures and Characterization of Specific Behaviors

The first modelization phase considers a single level structure which is defined on Fig. 2, in conformity with the UTCS technique specifications and the typical design rules of MCM-D technology. Essentially, the width and thickness of the copper interconnection lines are 20 and 2 μm respectively; the 8 μm high copper stud is assumed parallelipedic (30 μm $\times$ 30 μm); this simplifying assumption to traduce the real structure allows to simplify the FEM model meshing and does not influence the definition of the conductive thermal path. The thickness of the thinned die is 10 μm and the PTCB specific device considered is a multi-purpose test chip designed for experimental characterization of the thermal, electrical and reliability performance of chip packaging and interconnection technologies (current chip-on-board and flip-chip techniques more particularly) [9]. The lay-out of the 5 $\times$ 5 mm^2 unit cell illustrated on Fig. 3 includes two heating resistor areas (3900 $\times$ 1850 μm^2) symmetrically placed around the center of the chip and three diodes are used for temperature sensing.

The 3-D FEM thermal model was built with ABAQUS software [10]. The boundary conditions are on the one hand the fixed reference temperature—chosen to 0 °C—at the back side of the stacked structure, and on the other hand the adiabatic behavior for the top and lateral faces. Due to the uncertainties on the thermal conductivities of BCB and electroplated copper, and especially their variations with temperature, it was considered, for this first modeling phase, a linear thermal behavior by using the thermal conductance values reported in Table I. The other physical data also in this table will be used in the analysis presented in the following sections. We can note that the 0.18 W/m.K value retained for the BCB material is the pessimistic thermal conductance value given by the supplier (0.18 to 0.24 W/m.K range [11]). A characterization by thermoreflectance, at the micrometric scale [12] and on our

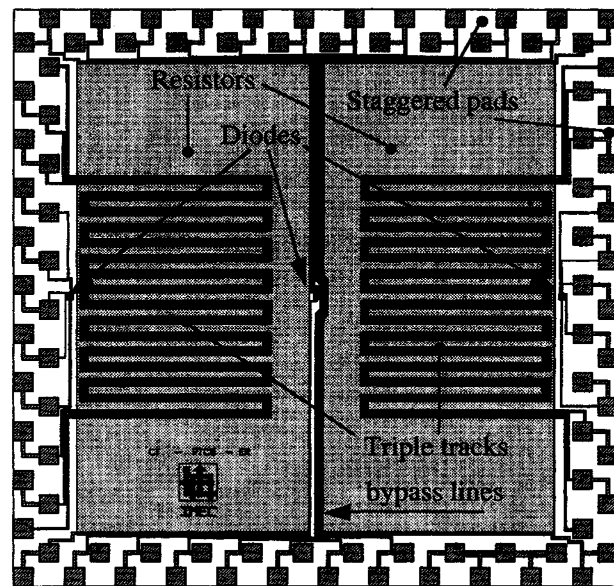

Fig. 3. View of the PTCB test structure.

TABLE I
Thermal Properties Overview of the Materials Used in the FEM Simulations

Material	Thermal conductivity (W/m.K)	Specific heat (J/Kg.K)	Density (Kg/m^3)
Si	117.5 - 0.42*(T-100)	836 + 0.121*(T+273) - 1.396*10^7/(T+273)^2	2330
BCB	0.18 – 0.24 [8]	1176 + 3.37*T [8]	1051 [8]
Cu	380	383	8900
Epoxy	1	300	2450
Al_2O_3	25	795	3800
Pb/Sn	36	137	11200
AlN	150	770	3260

specific samples, confirms this data and permits to verify also that the thermal transfer at the BCB/Si or BCB/Cu interfaces does not induce a significant limitation compared to the thermal resistance of the BCB adhesive layer with our technological species [13].

Fig. 4 shows the results obtained for a slice of the first level PTCB/carrier substrate that contains a single pad and its connection via a copper stud. It is clear that the thermal conduction occurs mainly through the thinned active PTCB chip, and that the essential part of the thermal resistance is defined by the conduction into the 3 μm thick BCB adhesive layer. An equivalent lumped thermal model established from a 1D conduction approach in all constitutive regions of the stacked structure with

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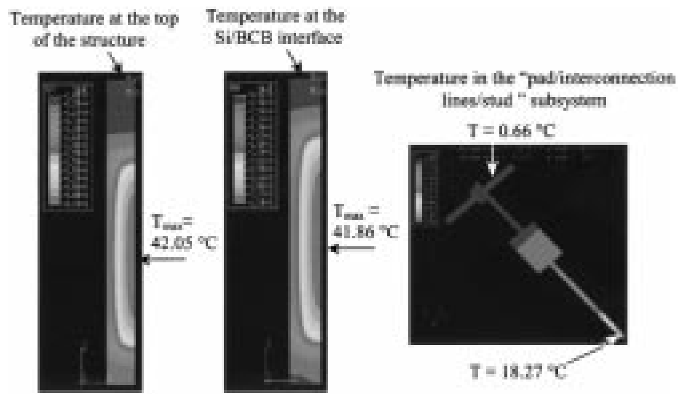


Fig. 4. Temperature distributions in one pair "stud/pad" slice from 3-D FEM.

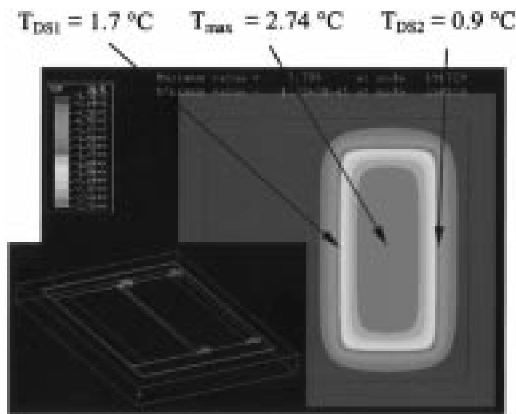


Fig. 5. Surface temperature contours of the PTCB single-level structure. Only one heat resistor is on and dissipates 1 W.

their connections allows an obvious interpretation of these observations.

A presentation of the simulated results now relative to the complete PTCB single-level structure previously described is given in the Fig. 5. As expected, the natural 3-D thermal conduction induces a temperature variation overall the surface of the heat resistor, and most particularly on the periphery. Here, for the particular use of the PTCB test device—which is the thermal characterization of the first stacked thin layers and not the layers of lower rank, as usual in the characterization of the packaging techniques—the temperature deviation between the hotter region and the diode sensor will not be neglected.

Apart the data necessary to the verification and the characterization of the single level test structure, these first modeling results (Fig. 5) give also a first evaluation of the heat transfer capabilities in UTCS technology. The obtained results show a value of the maximum temperature that leads to an apparent thermal resistance of 2.74 °C/W that can be compared to the 2.31 °C/W and 2.77 °C/W values calculated by considering a 1D thermal conduction through only BCB or a Si (10 μm)/BCB (3 μm)/Si (500 μm) tri-layers structure, respectively. If we consider uniform heat sources of great dimensions it appears that the limitation of the thermal transfer through a 3 μm adhesive BCB layer leads to an heating of five times higher than the one of the structure on its unthinned source substrate (500 μm thick).

The possibility to integrate, with this new technology, active devices with dissipating zones very confined thus presenting

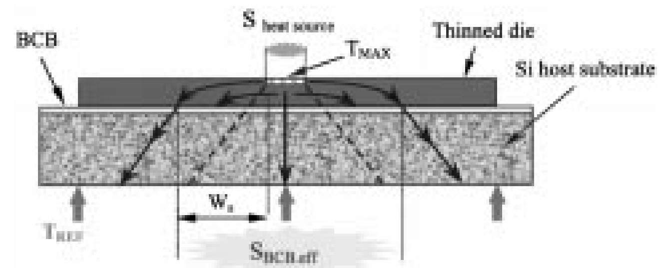
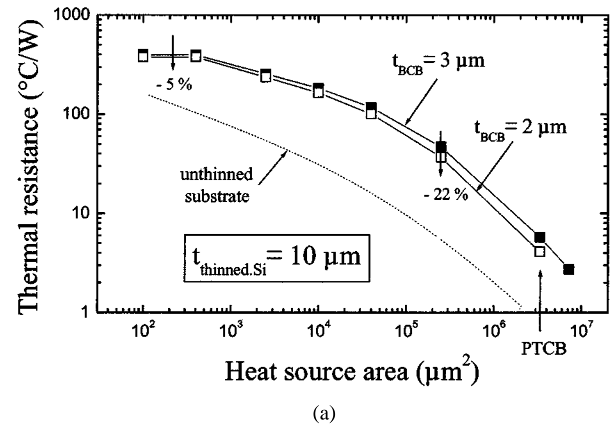
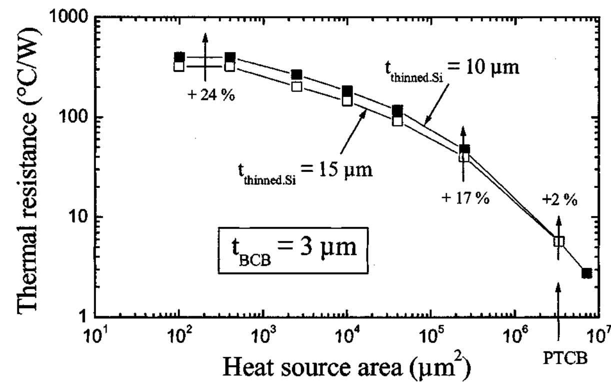


Fig. 6. Heat flux spreading mechanism in the "Si thinned die/ BCB adhesive layer/host substrate" stacked structure.



(a)



(b)

Fig. 7. Influence of heat source area on the apparent thermal resistance in the "thinned Si die/BCB adhesive layer/Si carrier substrate" stacked structure. Dependencies of spreading heat flux effects: (a) with BCB adhesive layer thickness and (b) with thinned Si die thickness.

reduced areas has been investigated. Here, the most affirmed 3-D character of the thermal conduction, with more particularly the influence of heat flux spreading in the Si thinned die with a very high conductivity compared to BCB (Fig. 6), leads to a saturation of the thermal resistance when the heat source area decreases as shown in Fig. 7. The simulation results show for an active area of 10 × 10 μm^2 an increase of the apparent thermal resistance compared to the unthinned device one with only a factor 2.4. However, the high related values obtained have to be considered with caution for the UTCS applications, because they'll fix the maximum temperatures that have to remain lower than the temperature allowable for functional and reliability limits. For the design rules optimization, we have calculated R_{TH} sensitivities to BCB adhesive layer and Si thinned

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die thicknesses, calculated as a function of the heat source area. The results illustrated on Fig. 7(a) and (b) show that

i) a reduction of BCB thickness gives an improvement with the same amplitude only for great areas, the domain where the thermal conduction has a quasi-1-D behavior;
ii) at the opposite, a die thinning limited to 15 μm rather than 10 μm (variation is 33% relative to 15 μm value) allows to benefit from the effects of heat spreading in the case of heat sources with small areas. A 24% decrease is calculated for thermal resistance in the saturated region where the effective dissipating section is quasifixed by the heat spreading mechanism.

III. Transient Thermal Characterization

Transient temperature measurement is the most suitable method for experimental characterization of packaging techniques [14], [15]. Indeed, the deduced thermal impedance function can be interpreted as a cross sectional view of the internal package heat flow structure that allows to well identify the different resistant components in the complete thermal path. This is all the more interesting as the matter is to well characterize the possible intrinsic thermal limitation in our new stacking technology.

As previously mentioned, the measured temperatures in the considered PTCB experimental test chip by means of diode sensors are underestimation values with respect to the actual temperature in the active heat resistor. This discrepancy can be important, in relative value, since the analysis of the thermal impedance is focused on the first phases of the thermal transfer, and can be an error source in the extraction of the relevant physical properties. To take into account this significant thermal decoupling between the heat resistor and the thermal sensor, it is therefore necessary to perform a true 3-D numerical simulation. Our FEM thermal modeling approach of the experimental set-up satisfies this requirement.

Transient experiments have been performed with a stacked structure mounted on DIL package. In the study the PTCB chip thinned down to 20 μm is glued to the carrier with a 3 μm BCB layer; the 600 μm thick silicon host substrate is attached on the alumina header of the package (760 μm thick) by means of the epoxy (50 μm). Measurements are performed in the environment of the laboratory with still air. One or two heating resistors of the test structure are activated under 2 W power each.

Fig. 8 gives a typical global response of the expected thermal impedance for this stacked structure: log-time representation shows clearly the separation of the sequential heat propagation times. The times range of interest in this transient analysis is limited to the small values (until ~100 ms for the heat transfer trough thinned PTCB chip, BCB attach layer and Si host substrate). Therefore, our 3-D model (restricted to the half structure) considers for the higher time values a simplified modeling approach by effective thermal transfer through epoxy attach layer, Al_2O_3 carrier and forced convection by backside only. The exchange area is 2.5×1.25 cm^2 and the reference temperature is 18 °C. A first fitting procedure with 3-D FEM simulation results, made in the first propagation time sequence by imposing a value of 0.2 W/m.K for thermal conductivity of

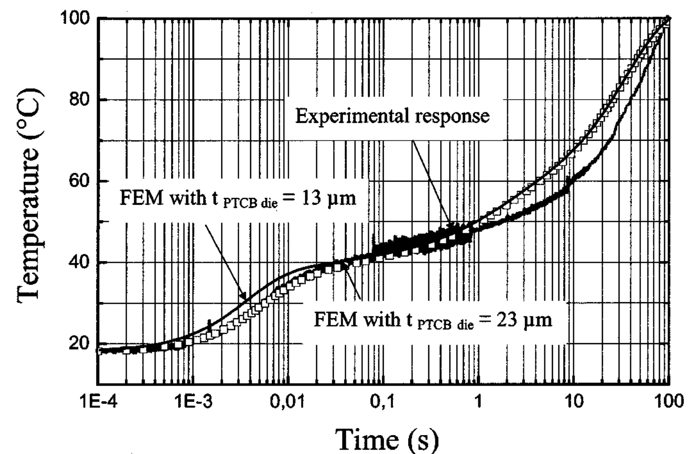

Fig. 8. Experimental and simulated transient temperature responses for the PTCB test device mounted in single-level UTCS structure.

BCB, gives extracted values of 23 μm and 1.3×10^4 W/m^2.K for the PTCB die thickness and the interfacial thermal conductance respectively. A second simulation procedure, considering now 13 μm for the thinned die thickness, shows a sensitivity of the transient response to this technological parameter. Finally, the effective heat transfer coefficient, relative to the modeling of natural convection in still air through a given equivalent surface carrier, is extracted in the high times range with a 70 W/m^2.K value.

This transient thermal characterization shows a significant limitation by BCB/Si interfacial conductances; the extracted value—1.3×10^4 W/m^2.K—defines an equivalent resistance which is in the order of four times higher than the one of the 3 μm thick BCB layer. A first estimation on one different study sample, under steady-state and on wafer probe station predicts only a 50% increase (the estimation gives an extracted interfacial thermal conductance value equal or greater than 3.5 $\times$ 10^4 W/m^2.K). Regarding this erratic behavior, one explanation may be found in the presence of sticking defects and their erratic localization related to temperature diode sensor. As a matter of fact, it is the transverse thermal transfer length in the thinned device which defines the sensitive area to the possible sticking defects. So, one device having only little and few defects near the diode sensor gives an apparent thermal resistance greater than the one with bigger defects but more distant of sensor.

IV. Heat Extraction Optimization by Interlevel Thermal Drains

Considering the results already obtained for the analysis of the thermal behavior in the one level structure, we have begun the study of the two levels stacking by considering directly the evaluation of the heat extraction by means of copper grid or full metal plate below the second level thinned chip, as is schematized in Fig. 9. For all the analysis made, we have considered the following parameters for the stacking:

1) Si carrier is 500 μm thick;
2) the thicknesses of the first and second thinned Si chips are 10 μm;

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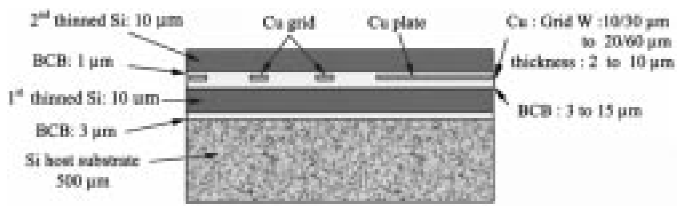

Fig. 9. Schematic view of the simulated two-levels structure with embedded Cu grid or Cu plate thermal drains.

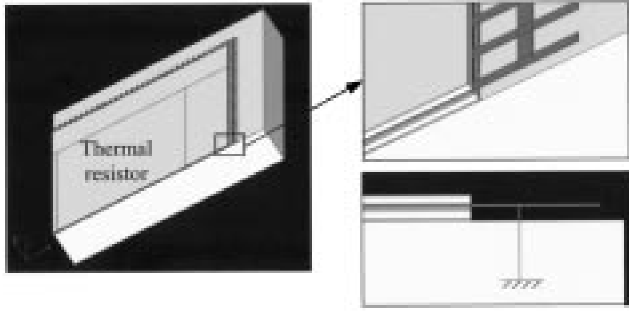

Fig. 10. Three-dimensional views of the quarter of two stacked PTCB structures embedding a Cu grid.

3) thickness of the first adhesive BCB layer is 3 μm;
4) thickness of the second BCB layer for planarization of first level is varied from 3 to 15 μm;
5) the width and spacing couple of the copper grid are varied from the W: 10 μm/S: 30 μm to 20/60 μm;
6) the thickness of the copper grid or the copper plate is considered in the 2–10 μm range;
7) finally, the third BCB layer for the adhesive of the second level chip is fixed to 1 μm.

In this first modeling step, the edges of either copper grid or copper plate are assumed to be at the reference temperature (the same as the host substrate temperature). Indeed, in this proposed new stack technology, the lateral heat extraction at the periphery of the structure will be ensured through copper via networks whose dimensions will be here much more favorable for the transfer if one considers the cross section and length of thermal path. It is thus allowed to neglect this contribution at this stage of the evaluation. Considering the double symmetry, into the X, Y plane, of two stacked PTCB, we have limited the 3-D numerical calculation to the quarter of the structure (Fig. 10). The surfacic density of dissipated power into the one, the other or both levels was considered at 14 W/cm^2 that corresponds to a power of 1 W into one thermal resistor.

Fig. 11(a) and (b) show the obtained isotherms onto the surface of the second level and onto the upper side of the copper grid for $W_{\rm Cu} = 20$ μm, $S_{\rm Cu} = 60$ μm and $t_{\rm Cu} = 2$ μm, for a single thermal excitation in the second level (called Heat$_2$). Fig. 11(c) compares the temperature plots on the axis of symmetry OX, for each one of the surfaces of the Si thinned chips located at the level 1 and 2, and for three thermal excitations heat$_1$, heat$_2$ and heat$_{1\,\rm and\,2}$. As expected for this study of the linear regime, the principle of superposition is verified and this is an interesting validation of our numerical results. Finally, still in the frame of the 3-D simulation of two stacked PTCB structures, Fig. 12 compares the behaviors for a copper grid, a full plate and the case where the metal was suppressed and replaced by a BCB layer of equivalent thickness (2 μm). These results induce two comments: firstly, in the center of the structure (corresponding to the heat resistance section) the substitution of BCB mater by metal with better thermal conductivity improves obviously the vertical thermal path; secondly, the lateral heat extraction by means of copper grid or full copper plate is only effective on the structure periphery, over a relevant distance $L_{T\rm eff}$ that we define as "effective transverse thermal transfer length."

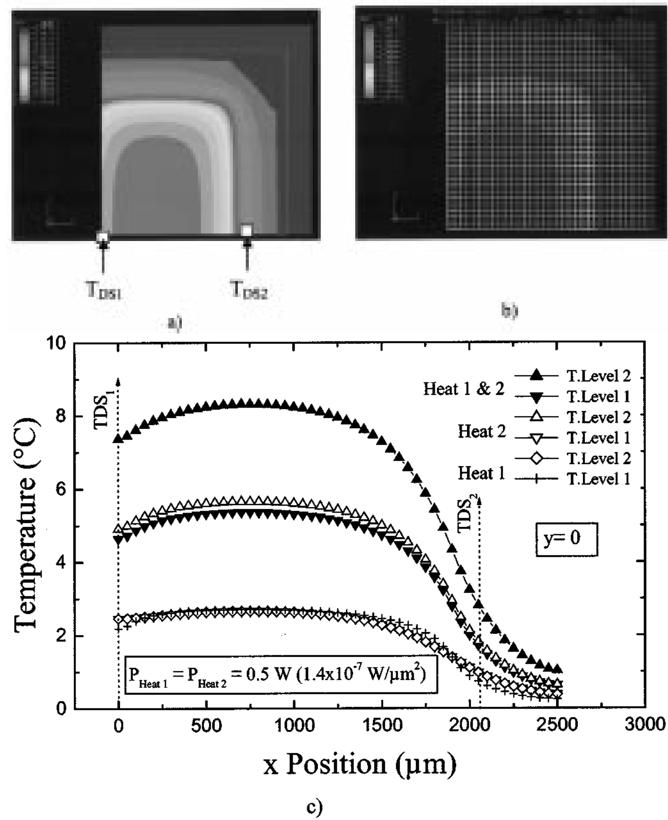

Fig. 11. Temperature distributions (a) onto the top of the second level and (b) onto the upper side of the Cu grid for heat$_2$ on and equal to 0.5 W. Superposition of the heat$_1$ and heat$_2$ effects is observed in temperature distributions calculated on (c) the Ox symmetry axis for each level.

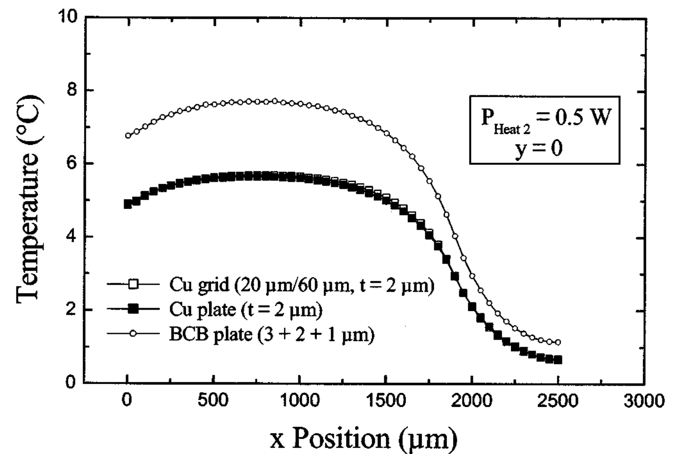

Fig. 12. Comparison of heat extraction efficiencies for copper grid or full copper plate having same thickness (2 μm).

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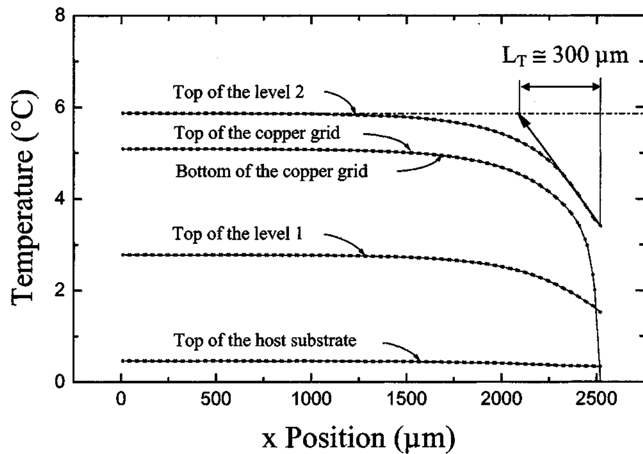

Fig. 13. Evaluation of the effective transverse thermal transfer length by a FEM modeling of one specific small slice.

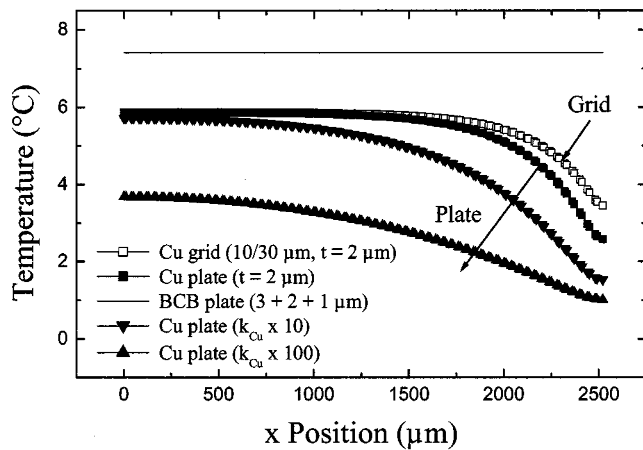

Fig. 14. Increase of heat extraction capabilities of embedded drains when the transverse component of the thermal resistance decreases.

To precise this behavior, particularly from a study of sensitivity to the different technological parameters, the 3-D calculation—which is too heavy—has been limited to only one slice. By another way the thermal dissipation is now considered uniform. Indeed, for our objective that is the evaluation of the lateral heat extraction capabilities, this simplification avoids the 3-D effects related to the delimitation of the heat source in comparison with the whole structure of the stacking. As an illustration of the obtained simulation results, for a copper grid having 20, 60, and 2 μm for width, spacing mesh and metal thickness respectively, the temperature plots all along the structure and for each stacking level reported on the Fig. 13 show the measurement of $L_{T\text{eff}}$. This distance is evaluated starting from the asymptotic variation of the temperature at the edge of the stacked structure. For the illustrated case, $L_{T\text{eff}}$ is around 300 μm and this model predicts a value of 1 mm when the couple 15 μm of BCB and 10 μm of Cu is considered. Finally, Fig. 14 compares the lateral heat extraction capabilities respectively for the grid and full plate, as well as the thickness of metal plate effects mimed through thermal conductivity values. As expected, the increase of $L_{T\text{eff}}$ do not follow linearly the decrease of the transverse resistance component of the heat spreader. One can easily interpret this behavior by means of a "Transmission Line Model" based and simplified approach: the estimation of the transfer length, which permits to predict a tendency, is given by the following relationship:

$$L_T = \sqrt{\frac{k_{\text{Cu}} \cdot t_{\text{Cu}} \cdot t_{\text{BCB}}}{k_{\text{BCB}}}}. \tag{1}$$

It is clear that, for the structural parameters compatible with UTCS design rules, the effective transverse thermal transfer length will be small relatively to the usual die size. However, this technique can give an interesting improvement of the thermal path because in integrated circuits, the buffer devices dissipating most of the power are generally localized in this peripheral zone. Obviously, the efficiency and the interest of this extraction technique would be increased if BCB conductivity and/or BCB/Si interfacial thermal conductance would be highly altered with respect to expected properties. By allowing the heat flux spreading in the regions where the attachment is poor—voids or bubbles in the BCB adhesive layer essentially—they will contribute to the temperature uniformization. Fig. 15 illustrates a study of this improvement of capabilities by comparing the effects of three voids of 500 $\times$ 500 μm^2, 250 $\times$ 250 μm^2 and 100 $\times$ 100 μm^2 respectively, for a copper grid and copper plate of 2 μm thick embedded in a 3 μm BCB adhesive layer. In agreement with the thermal transfer length value estimated previously for the corresponding technological configuration—$L_T \sim 300$ μm—we observe that the metal plate is really useful to spread heat flow and make uniform the temperature if the void size is lower than 500 μm.

V. Thermal Evaluation of Space Demonstrator

For the feasibility demonstration of this new ultra-compact chip stack technology we have retained a subsystem for space application. This first demonstrator, currently under development and described in [16], is a channelizer prototype including three cascaded ASICs having 1.5 $\times$ 1.5 cm^2 size with 450 I/O each and dissipating 3.8 W at 33 MHz bus speed.

The aim of the present study is the research and the evaluation of the better packaging efficiency in terms of the higher degree of integration remaining compliant with spatial thermal specifications (range of allowed temperatures 90–110 °C). The main specifications and characteristics retained for this study could be summarized as follows.

i) As schematized in the Fig. 16 UTCS structure is mounted on PGA package with AlN header and temperature case is maintained at the temperature board (70 °C) with only thermal conduction based regulation; a three levels stacking involves 13 μm thinned dies and 13 μm adhesive BCB layers; for worst case estimation, we have considered five interfaces (BCB/Si, BCB/Cu and BCB/BCB interfaces) with their relative thermal conductance.

ii) We have examined the thermal behavior of the four main alternatives stacking procedures illustrated on the Fig. 17: Stacking with a precise overlapping of three dies on three levels (stack S_1), and stacking on two or three levels with overlapping between dies by half (stacks S_2, S_3 and S_4).

Starting from the conclusions of previous analysis our approach for this thermal modeling relies on three essential considerations.

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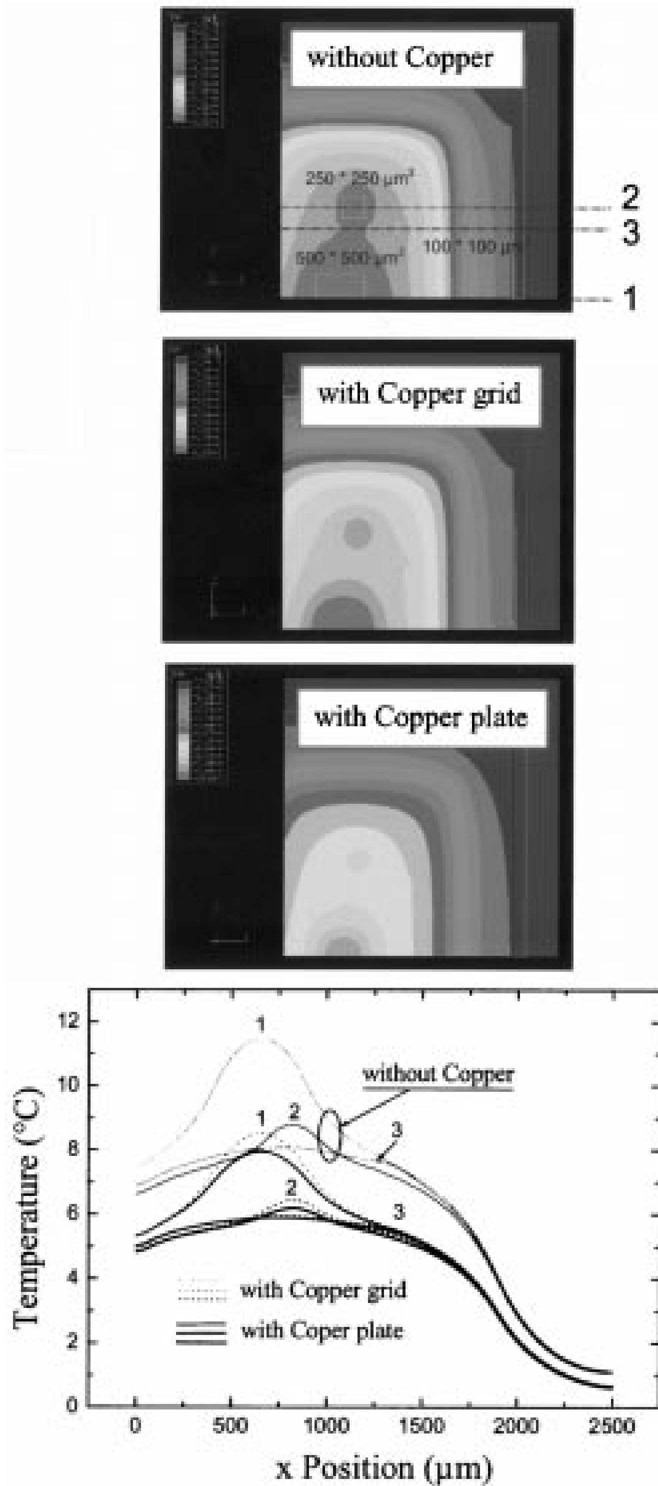

Fig. 15. Evaluation of thermal extraction capabilities of Cu grid or Cu plate for the prevention of sticking defects through the study of void size influence.

1) One-dimensional thermal conduction model is a good approximation for these large active devices with uniform dissipated power.
2) Thermal effects relative to SiO_2 layers and metallic interconnections in processed area of the thinned dies have been ignored; indeed, starting from $k_{\mathrm{Sio2}} \cong 2$ W/m.K and $k_{\mathrm{BCB}} \cong 0.2$ W/m.K, 1 μm of SiO_2 layer has the same effect than 0.1 μm of BCB and the very small size of interconnection lines minimizes the thermal transfer.

Fig. 16. Main stacked technology specifications for space demonstrator evaluation.

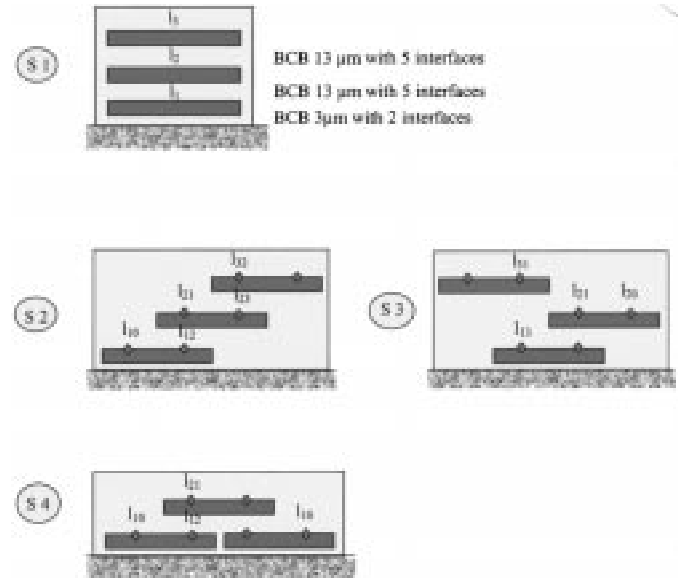

Fig. 17. Schematic stacking procedures which are considered for space demonstrator evaluation.

3) Linear regime is considered; thus the principle of superposition can be applied and the temperature increase of devices can be estimated independently of reference case temperature; with these conditions the analytical approach is given by the following procedure.
   a) Self-heating of the active device in the "i" level of the "n" levels stacking structure is

$$\Delta T_i(x, y) \approx \left[0.05\,^\circ\mathrm{C} * t_i(x, y) + \frac{1\,^\circ\mathrm{C}}{k_{\mathrm{interface}}} * n_i(x, y)\right] * p_{d_i}(x, y). \quad (2)$$

   b) The temperature increase in the "i" level of the "n" levels stacking structure is then given by the relationship

$$\Delta T_i^n(x, y) \approx \left[0.05\,^\circ\mathrm{C} * t_i(x, y) + \frac{1\,^\circ\mathrm{C}}{k_{\mathrm{interface}}} * n_i(x, y)\right] * \sum_{\alpha=i}^{n} p_{d_\alpha}(x, y) + \sum_{\beta=1}^{i-1} \left[0.05\,^\circ\mathrm{C} * t_\beta(x, y) + \frac{1\,^\circ\mathrm{C}}{k_{interface}} * n_\beta(x, y)\right] * p_{d_\beta}(x, y) \quad (3)$$

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TABLE II
COMPARISON OF THERMAL BEHAVIOURS CALCULATED FOR THE DIFFERENT STACKING TOPOLOGIES OF THE THREE-LEVELS SPACE DEMONSTRATOR. DISSIPATED POWER IN EACH LEVEL IS 4 W (1.78 W/cm^2)

Stack characteristics				Total temperature increase (°C)		
Stack	Level	t_{BCB} (µm)	Num. of Inter.	$k_{inter} = \infty$	$k_{inter} = k_{i1}$	$k_{inter} = k_{i2}$
S_1	l_3	29	12	4.25	15.4	32.9
	l_2	16	7	3.1	11.6	24.9
	l_1	3	2	0.8	4	9
S_2	l_{32}	42	12	6.3	16.4	32.2
	l_{31}	42	12	4	11.4	23.1
	l_{30}	55	12	4.9	11.2	21.2
S_3	l_{23}	29	7	5.1	12.6	24.2
	l_{21}	16	7	1.7	6.5	13.9
	l_{20}	29	7	2.6	6.3	12.1
S_4	l_{13}	3	2	0.5	2.65	6
	l_{12}	3	2	0.5	2.65	6
	l_{10}	3	2	0.3	1.3	3

where $t_i(x, y)$ is the cumulative thickness (expressed in μm) of BCB layers under "i" level at the (x, y) position, $n_i(x, y)$ is the number of BCB/Si interfaces under "i" level at the (x, y) position, and $p_{di}(x, y)$ the dissipated power density (expressed in W/cm^2) in the "i" level at the (x, y) position.

The corresponding results for this projection are reported in Table II. In this evaluation, we have considered three values of interfacial thermal conductance: $K_{\text{inter}} = \infty$ supposing a perfect thermal transfer at each interface, $k_{i1} = 3.5 \times 10^4$ W/m^2.K extracted by preliminary steady-state thermal characterization of thinned PTCB chip in single level UTCS test structure on wafer probe station, and $k_{i2} = 1.3 \times 10^4$ W/m^2.K extracted by fitting a experimental transient response with 3-D simulation results. The part of thermal resistance relative to the heat transfer through successively the silicon host substrate, the Pb/Sn solder and the AlN header, estimated by 1-D approach, induces a temperature increase of about 0.6 °C. Assuming 70 °C case temperature, it appears that the hottest point will not be higher than 104 °C in worst case, which makes the S_1 stacking structure compliant with space specifications, with the better packaging efficiency in terms of degree of integration. It is also important to observe for each level a maximum temperature increase practically equivalent to the one observed for other S_2, S_3 and S_4 stacked devices. Indeed, for shifted stacking, the thermal coupling effects between the different levels are replaced by a self-heating mechanism through a most resistant thermal path (the cumulative layer thickness of the poor conductor BCB is higher). Finally, one can note a smaller temperature increase in the S_1 package which not exceed 5 °C when the good thermal transfer at the interfaces is considered.

VI. CONCLUSIONS

The new ultrathin chip stacking technology has been evaluated on the point of view of the thermal performance. A 3-D FEM model was first used to confirm the expected heat flow distribution and transfer limitation by the BCB adhesive and planarization layers inserted between thinned active devices. A study of sensitivity to the size of the heating area has shown that devices dissipating a high power density have to be considered with caution. Indeed, for example, for a 10×10 μm^2 device transferred on 3 μm of BCB adhesive layer, the apparent thermal resistance becomes 2.4 times higher than the one of the unthinned structure, in spite of a beneficial effect of the heat spreading in the high conductive thinned device. It is clear that with this stacking process the possible power systems will be located into the first level.

The first experimental characterizations by the thermal transient method have benefit from the accuracy provided by 3-D FEM calculations, essentially to well account for thermal decoupling between heating resistor and diode sensor in the used specific test chip.

For the objective of the design optimization of this new packaging technique, our true 3-D modeling approach, with a parameter sensitivity study, allowed to quantify the thermal transfer improvement brought by the embedding of copper grid or plate between the stacked thin chips. Heat extraction enhancement is advantageous

1) for the vertical heat transfer since the metal replaces a part of BCB;
2) for the temperature uniformization into the possible sticking defects areas thanks to its heat spreader capability;
3) by adding lateral conduction path at the peripheral zones of the stacked structure.

The technological constraints, and probably the electrical added function (ground plane notably), will direct the choice of either solution by imposing some inevitable tradeoffs.

Finally, all conclusions of this presented modeling study are used for the quantitative projections of the thermal performance of a first demonstrator based on a three-levels stacking structure for space application and currently under development. It is shown that the most compact stacking structure among the considered options remains compliant with spatial thermal specifications.

ACKNOWLEDGMENT

The authors would like to thank W. Claeys and Dr. S. Dilhaire, Bordeaux University (CPOH), for material characterization by thermoreflectance measurements.

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Stéphane Pinel received the B.S. degree from Paul Sabatier University, Toulouse, France, in 1997, and the Ph.D. degree in microelectronics and microsystems from the Laboratoire d'Analyse et d'Architecture des Systemes, Centre National de la Recherche Scientifique, Toulouse, in 2000.

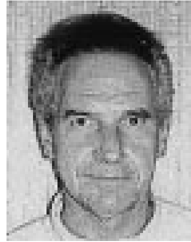
He has worked on a UltraThin Chip Stacking (UTCS) European Project for three years and is currently a post-doctorate in the Microwaves Applications Group, Georgia Institute of Technology, Atlanta. His research interests include 3-D integration and packaging technologies, RF packaging, and SOI RF circuit design.

Antoine Marty received the D.Eng. and D.Sci. degrees both from the University Paul Sabatier, Toulouse, France, in 1974 and 1980, respectively.

Since 1976, he has been at the Laboratoire d'Analyse et d'Architecture des Systèmes du Centre National de la Recherche Scientifique, Toulouse. His main research activities are in physical modeling, design optimization, processing, and characterization of AlGaAs/GaAs heterojunction bipolar transistors-based high-frequency and/or high-power and photodetector devices, and digital integrated circuits. His latest research interests include the thermal management of transferred power HBTs and innovative 3-D packaging technologies.

Josiane Tasselli received the M.S and Ph.D degrees in electrical engineering from the University Paul Sabatier in Toulouse, France, in 1983 and 1986, respectively.

At LAAS-CNRS since 1988, her research concerned the fabrication of GaAlAs/GaAs and GaInP/GaAs heterojunction bipolar transistors for power applications. Her present work focuses on microsystems and involves the design and fabrication of microfluidic devices such as microvalves and micropumps. She also is interested in the study of new 3-D integration techniques.



Jean-Pierre Bailbe was born on June 1946. He received the D.Eng. and D.Phys. degrees from the Faculté des Sciences of Toulouse, France, in 1969 and 1977, respectively.

He is Directeur de Recherche, CNRS. He has worked on physical modeling, optimization and realization of bipolar transistors first in silicon then in gallium arsenide. His present works concern the realization of 3-D devices with ultra thinned stacked components.

Eric Beyne was born in Tienen, Belgium, on May 26, 1960. He received the M.S. degree in electrical engineering and the Ph.D. degree in applied sciences from the University of Leuven, Belgium, in 1983 and 1990, respectively.

From 1983 till 1985, he was a Research Assistant at University of Leuven. In 1986, he joined IMEC, where he worked on his Ph.D. on the interconnection of high-frequency digital circuits. He is presently head of the High Density Interconnection and Packaging Group, IMEC.

Dr. Beyne is Secretary of the IMAPS-Benelux Committee.

Rita Van Hoof received the B.S. degree in biochemical engineering from the KIH De Nayer, St. Katelijne Waver, Belgium, in 1986.

In 1988, she joined IMEC, Leuven, Belgium. Since 1990, she has worked on thin film processing issues for MCMs.

Santiago Marco received the M.S. degree in physics and the Ph.D. (with honors) degree in the development of a novel silicon sensor for *in-vivo* measurements of the blood pressure from the Departament de Física Aplicada i Electrònica, Universitat de Barcelona, Spain, in 1988 and 1993, respectively.

He has been Associate Professor at the Departament d'Electronica, Universitat de Barcelona, since 1995. From 1989 to 1990, he was working in the electro-optical characterization of deep levels in GaAs. From 1990 to 1993, he was a regular visitor of the Centro Nacional de Microelectrònica, Bellaterra, Spain. In 1994, he was Visiting Professor at the Universita di Roma "Tor Vergata," Italy, working in data processing for artificial olfaction. He has published about 40 papers in scientific journals and books, as well as more than 80 conference papers. His current research interests are twofold, chemical instrumentation based on intelligent signal processing and microsystem modeling by FEM and HDLA languages.

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Joan Ramon Morante received the Ph.D. degree in physics from the University of Barcelona, Spain, in 1980.

He joined the Department of Applied Physics and Electronics, University of Barcelona, in 1977, and in 1986, was appointed full-time Professor of electronics in this Department. The same year, he founded the Laboratory of Characterization of Materials for Microelectronics (LCMM). In 1991, he founded the Electronic Materials and Engineering Research Group (EME). He is now head of this laboratory and co-Director of the Microsystem Engineering Centre, CEMIC. His current research activities and projects are centered on characterization of electronics materials and microtechnological and nanotechnological processes, micromechanics, sensors, actuators, microsystems, gas sensors, and semiconductors devices. He is author or co-author of more than 400 scientific and technical papers.

Olivier Vendier received the M.S. degree in applied physics from the Institut National des Sciences Appliquées, Toulouse, France, in 1993 and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology (Georgia Tech), Atlanta, in 1997.

From 1993 to 1997, he was an R&D Engineer at the College of Electrical Engineering, Georgia Tech. His research expertise was optical interconnects for 3-D high throughput systems. As a member of the Packaging Research Center he was involved in several projects associated with high density packaging (quasi-monolithic integration) for RF applications. Starting from Fummer 1997 he was part of the Technical Staff, Technology Department, Alcatel Space Industries, where he was involved in various advanced packaging based projects. He is now with the RF Product Department, Advanced Microwave Study Group, where is heading two IST projects and is starting RF MEMS activities for the department. He has published over 35 papers in various journal and conferences and holds three patents.

Marc Huan, photograph and biography not available at the time of publication.

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