the presence of yttrium in the PS Matrix. Fig. 2 exhibits the EDS analysis spectra of the as-prepared PS layer confirming also the presence of the incorporated yttrium oxide into the porous silicon layers, before annealing.

Fig. 3 shows the variation of the Skewness (S_{sk}) and the average maximum profile valleys depth, deduced from AFM analy²sis. They are important in giving a better understanding of the surface. Skewness (S_{sk}) is a measure of the asymmetry of the distribution of heights about its mean line, when it is symmetrical its value is zero. Negative values of S_{sk} indicate that the surface is more planar and valleys are predominant. In fact, if the surface has more peaks than valleys and the height distribution is asymmetrical the Skewness is positive [16, 17].
Accordingly, as shown in fig. 3, the obtained values of S_{sk} prove that the surface contains a high concentration of pores that tend to decrease after annealing the immersed samples. This is due to the pore filling with yttrium oxide that took place after increasing the annealing temperature to 500 °C, then S_{sk} decreases obviously. The decrease of the skewness for higher temperatures can be related to the diffusion of the incorporated yttrium oxide deep into the pores due to the thermal treatment effect [13, 14].

Due to the importance of the textured surface analysis to study the morphology of the prepared samples, we plotted the variation of the average maximum profile valley depth (R_{vm}) in fig. 3. The latter is defined as the measure of the deepest pore (described as valley) depths in the yttrium-treated porous silicon, calculated over the surface [16, 18, 19]. It concerns the deepest valleys across the surface profile analyzed from the mean line. R_{vm} is a useful parameter to study the morphological changes in the post-annealed yttrium/PS layers. According to fig. 3, R_{vm} variations indicate an apparent dependence of the pores (described as valleys) dept with annealing temperature due to the induced agglomerations and pore filling that looks in accordance with the discussed variations of the skewness (S_{sk}).
Fig. 4 shows the photoluminescence dependence of porous silicon with the subjected yttrium passivation post-annealed at different temperature. The PL intensity increases first and then decreases drastically as the temperature exceeds 600°C. It can be seen that the highest improvement in the PS photoluminescence was obtained after the passivation of PS with yttrium oxide thin film after post-annealing at 600°C. The PL intensity of PS is increased significantly compared to that of the uncoated PS.

The total reflectivity was measured by means of Perkin-Elmer Lambda spectrophotometer equipped with an integrating sphere. Fig. 10 shows the reflection spectra for the as-prepared untreated PS, the as-deposited yttrium oxide onto the PS layer and the post-annealed yttrium–PS at the optimum temperature 600°C. It can be seen that the reflectivity of the PS layer was reduced to its lower values after annealing at 600 °C. The increase of temperature leads usually to a variation of the morphology, which notably reduces the reflectivity. The reduced reflectivity can be partially explained by an increased roughness after the incorporation of yttrium oxide into the PS layer. It is well known that surface morphologies with high roughness, allowing a high scattering and therefore a resulting low reflectivity. This behavior is mainly attributed to the high internal multiple reflections into the porous structure, as illustrated in fig. 9 (a), known to trap efficiently the incident light.

The combined effect of the post-annealed yttrium/PS at various temperatures acts as a passivating layer of the crystalline silicon surface and also an efficient antireflection layer increasing consequently the absorption of the incident light at the front surface. The latter was investigated by means of the Internal Quantum Efficiency (IQE) and the effective minority carrier lifetime measurements. Results show clearly the effect of yttrium oxide on the passivation process of the PS layers and its dependence with temperature, compared with the as-prepared untreated PS subjected to the same thermal treatment in the same conditions. The effective minority carrier lifetime shows a minor improvement in the as-prepared untreated PS layers subjected to the same thermal annealing, as shown in fig. 11, with maximum values not exceeding 8 μs. Concerning The PS/Yttrium treatment post-annealed at various temperatures, measured τ_{eff} reach its highest values 37 μs after annealing PS/Yttrium at 600°C, showing a good agreement the discussed results in the PL study. Thus, carrier lifetime was significantly improved by the proposed Yttrium-PS treatment, in view of the fact that recombination activities have been reduced significantly allowing the obtained increase of the effective minority carrier lifetime. Lee and Glunz [28] showed that improve carrier lifetime also improved the solar cell efficiency. This was reported in many previous works since improving the electrical properties of crystalline silicon is of great importance for photovoltaic applications [29, 30].

In point of fact, the front surface reflectance can be reduced by means of texturization, but due to an increase in the number of surface defect states the recombination activities will rise. In view of that, the proposed yttrium-passivation treatment of PS layer, grown at the front surface, aims to reduce the recombination activities and to improve the surface quality. As

discussed, obtained results prove the beneficial effect of the deposited yttrium oxide which passivated the surface defect states efficiently. To investigate furthermore the effect of yttrium-PS treatment we measured the internal quantum efficiency (IQE) after each thermal annealing, presented in fig. 12. An internal quantum efficiency spectrum can be defined as an involvement of the known three parts of a pn junction, namely the emitter, space charge and base [31]. Wavelengths less than 600 nm can penetrate only up to a few micrometers into the silicon substrate, consequently, a large number of charge carriers in the emitter and close to the pn junction regions will be generated. The recombination activities at the front surface in silicon has a significant effect on the generated carriers collection probability in the short wavelength range, since it is well known that recombination has a detrimental effect on the electrical properties of silicon solar cells. According to the IQE spectra, in fig. 12 it is apparent that the major difference between the annealed samples appears in the wavelength region 400 − 650 nm, confirming that 600°C is the optimal annealing temperature and found to be consistent with our discussed results. Improvements are also significant between 650 and around 900 nm, indicating an obvious improvement of the electrical properties in the bulk. The effect of yttrium-PS passivation through a thermal annealing enable a non negligible thermal agitation of impurities to facilitate its migration near the surface were they will be trapped into the porous silicon layers and at the interface, which increases the recombination activities, as illustrated in fig. 9(b). The latter can explain the PL drop after annealing at 700°C and seems to be in good agreement with the variations of the effective minority carrier lifetime of fig. 11.

Conclusion

In order to gain insight into the porous silicon properties after the yttrium-PS treatment, we studied the effects of thermal treatment and aging in air ambient. The deposited yttrium oxide exhibits a crucial role on the stabilization of PL during aging and improves its intensity after a post-annealing at an optimum temperature, which was found 600°C. Obtained results prove the beneficial effect of yttrium-PS passivation on the PL properties of porous silicon and its effect on the improvement of the electrical properties in the corresponding crystalline silicon substrate, regarding essentially the important improvement of the effective minority carrier lifetime that reached 37 μsec after annealing at 600°C, and the IQE measurements. Hence, yttrium oxide incorporation into porous silicon is a promising process for porous silicon to realize enhanced silicon-based optoelectronic devices.

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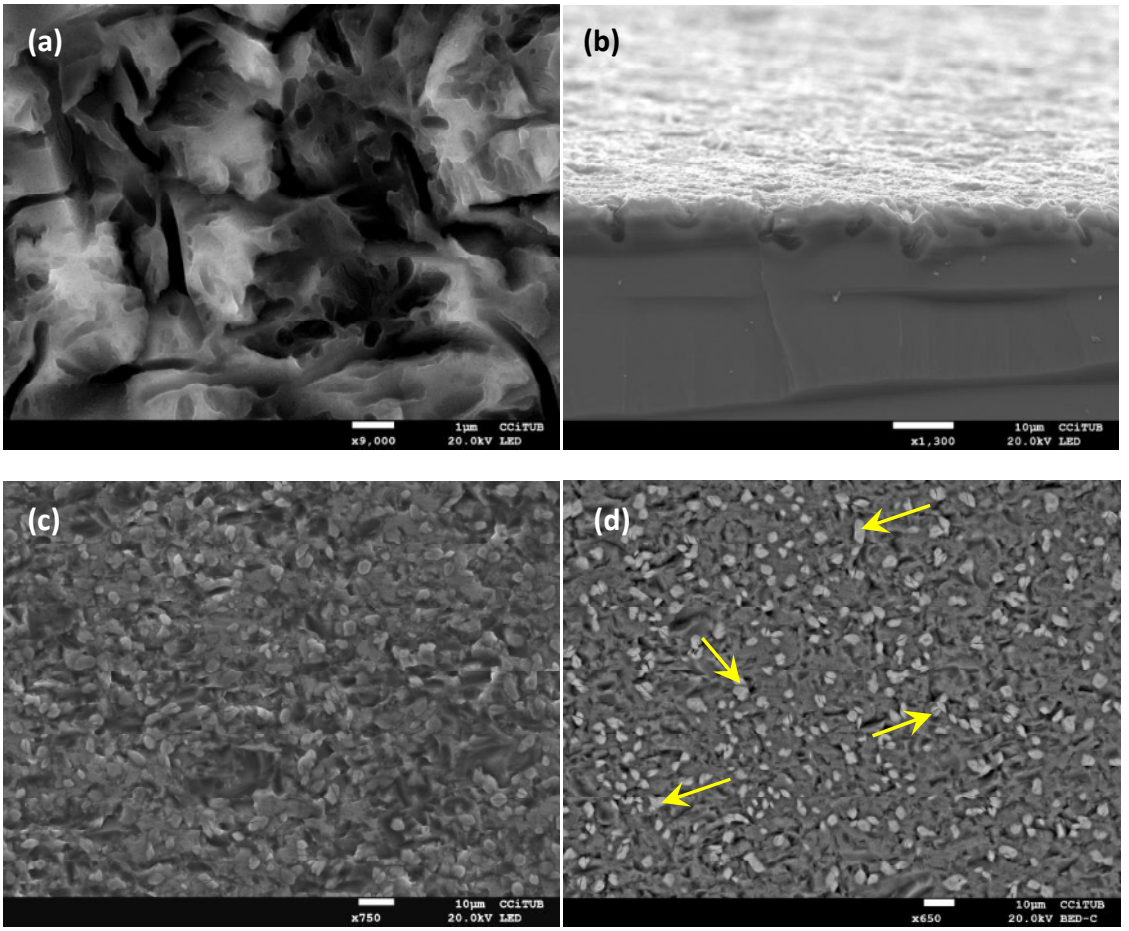


Fig. 1. SEM micrograph of the PS structure (a), cross-sectional view (b). (c) and (d) are the same sample with different imaging mode: The lower electron detector (LED) and the Backscattered Electron Detector (BED-C) for composition imaging and analysis, respectively. (d) shows the deposited yttrim oxide nanocrystallites appearing in light gray randomly distributed onto the PS layer (marked using some yellow narrows).

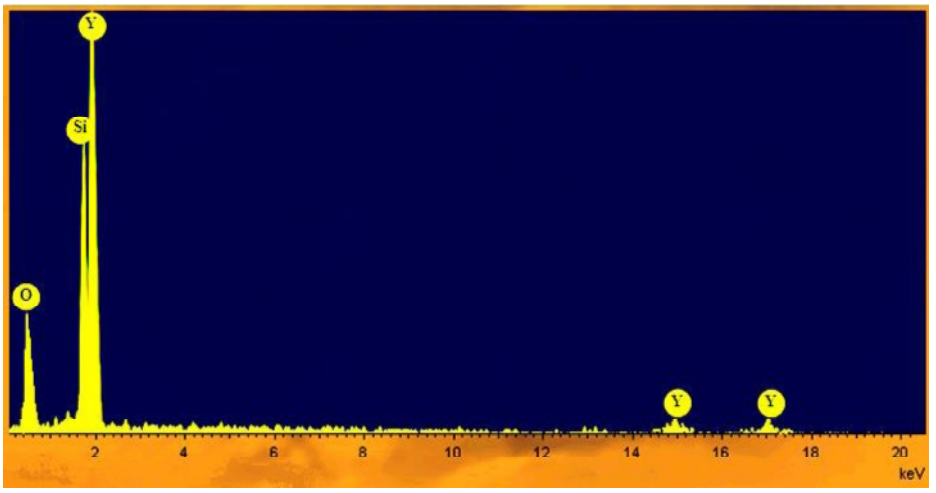


Fig. 2. Energy dispersive spectroscopy (EDS) analysis of the as-deposited yttrium oxide onto the PS layers.

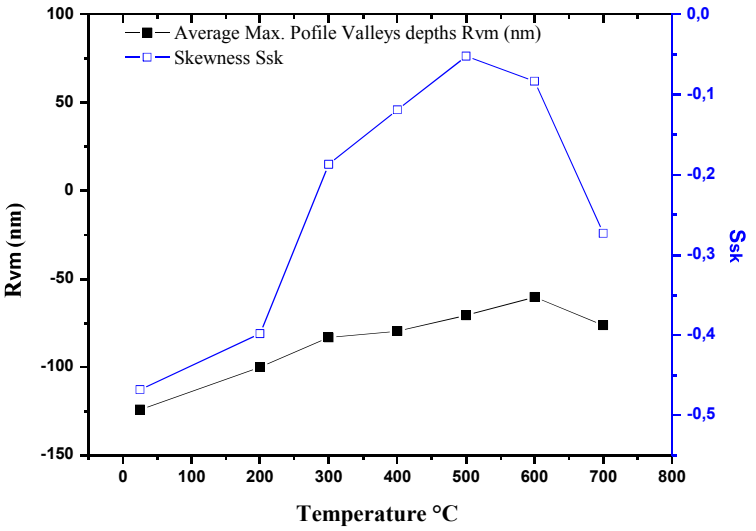


Fig. 3. Average roughness parameters of the treated porous silicon layers, deduced from AFM surface analysis: Pores depth variations and morphology profile.

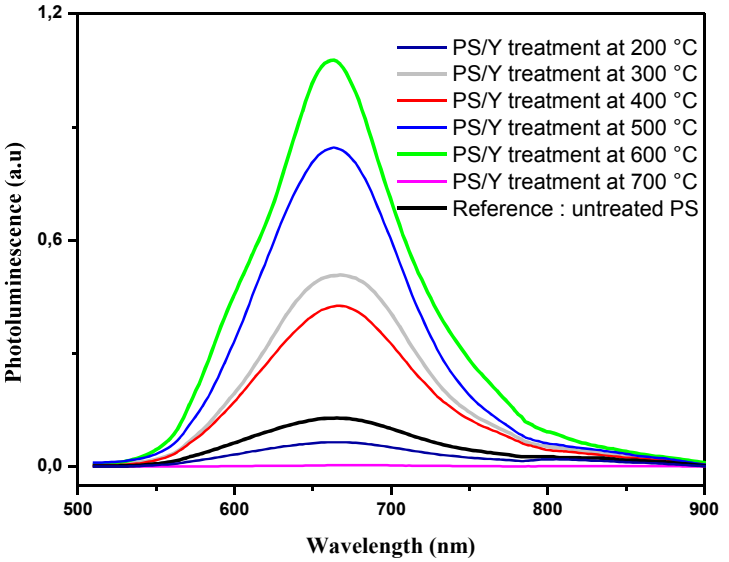


Fig. 4 PL spectra of the Yttrium-PS passivated layers annealed at different temperatures.

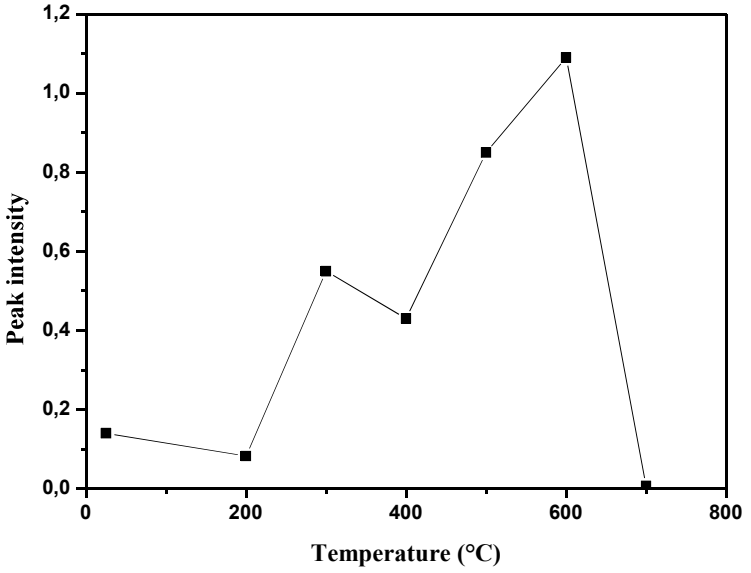


Fig. 5. Photoluminescence peak intensity dependence with thermal annealing after the yttrium-PS passivation.

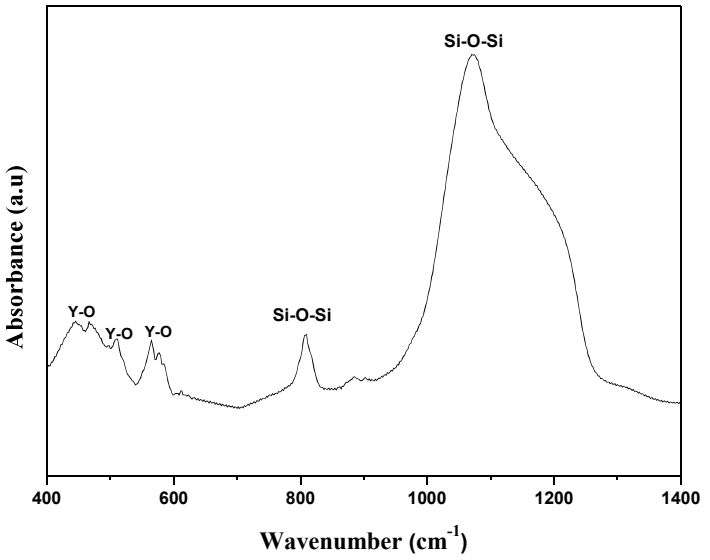


Fig. 6. FTIR spectra of the treated Y/PS layer at the optimum annealing temperature 600°C.

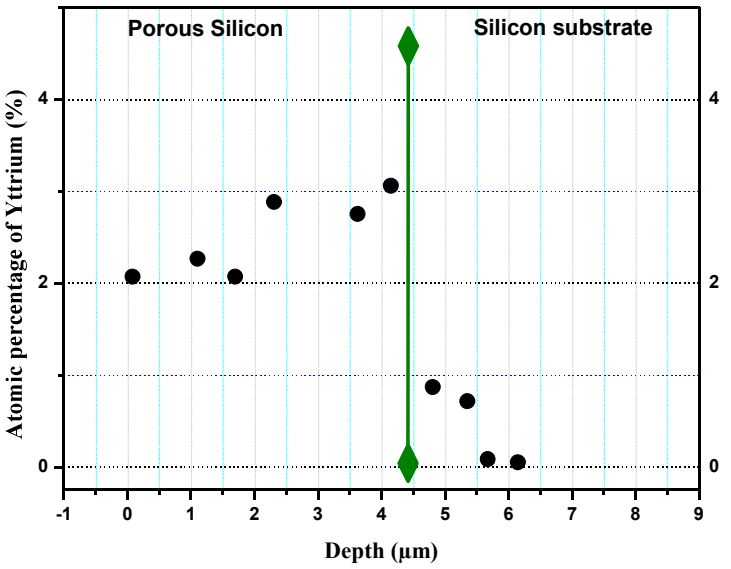
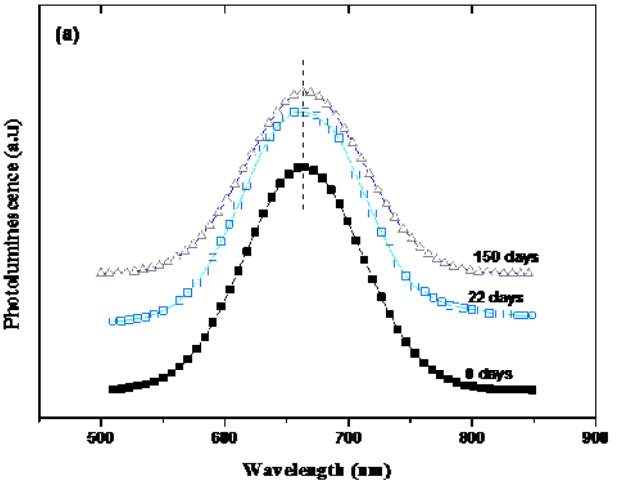


Fig. 7. Atomic percentage of yttrium obtained from a cross-section analysis, in different regions after annealing at the optimum temperature 600°C, using EDS analyses.



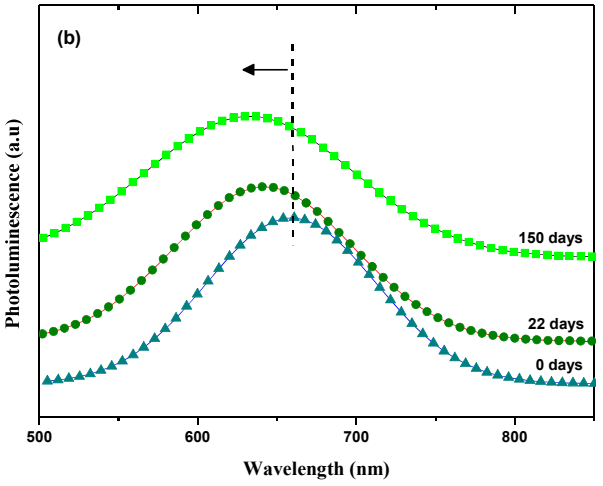


Fig. 8. Photoluminescence spectra of PS/Y annealed at 600°C (a), and the as-prepared untreated PS (b), after aging for 22 and 150 days.

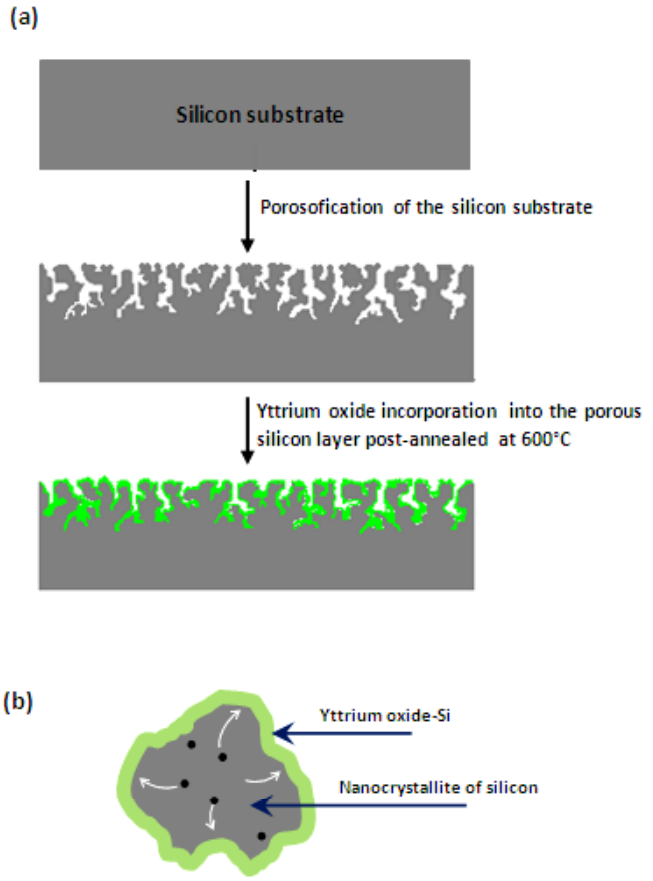


Fig. 9. Schematic illustration of the obtained formed porous silicon (a) and the effect of the thermal annealing on the migration of some impurities toward the outer surface of nanocrystallites allowing a further reduction of the recombination activities in the PS layer (b).

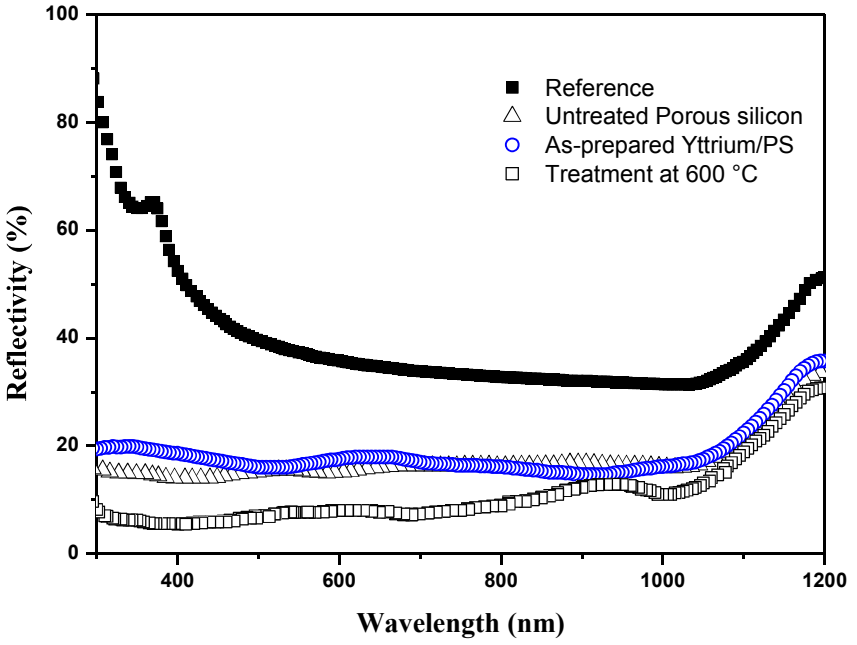


Fig. 10. Total reflectivity spectra showing the difference between an as-prepared untreated PS layer, the as-deposited yttrium oxide onto PS and the post annealed yttrium-PS at the optimum annealing temperature (600°C).

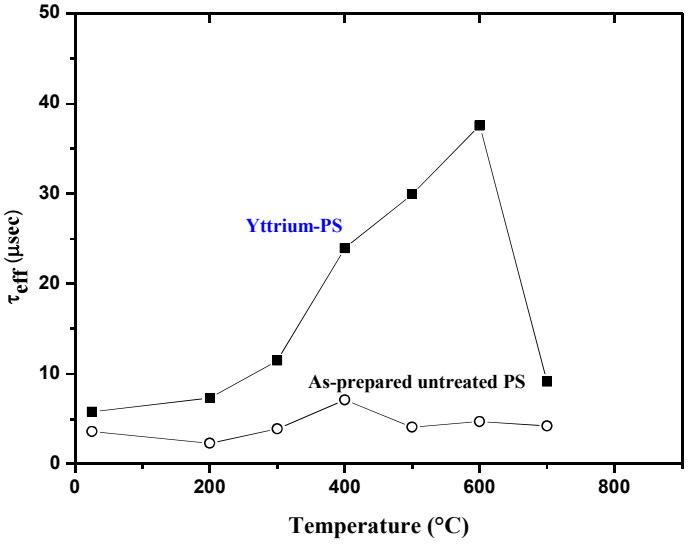


Fig. 11. Temperature dependence of the effective minority carrier lifetime τ_{eff} in the yttrium-PS passivated layer compared to an as-prepared untreated PS layer subjected to the same thermal treatment.

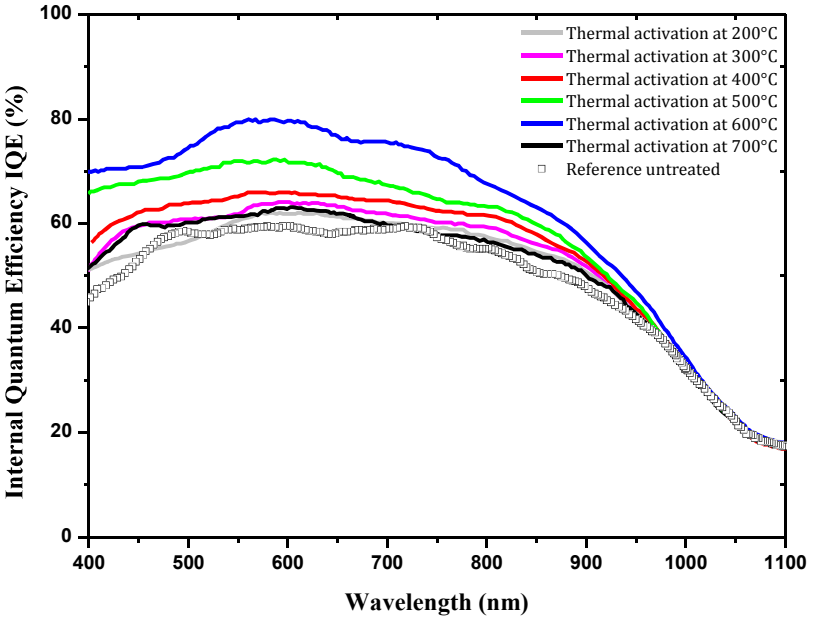


Fig. 12. Internal quantum efficiency (IQE) variations of the treated PS layers with yttrium oxide compared to a reference untreated sample.