# Resistive switching properties of $SiO_2$ with embedded Si nanocrystals

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**Abstract**: In this paper, a layer of $SiO_2$ is studied, in hopes of measuring its characteristics, how the resistive switching is produced in this material and how its performance could be improved. A middle ground resistance state has been hinted in our device, which could be used for neuromorphic applications, but attempting to stabilize this state was impossible. Even so, our devices performed well during more than 200 sweeping cycles, and more than 1000 pulse cycles when the maximum electrical current to the device was limited to 100 μA. The low resistance state of our material was maintained for up to two days, proving the state stability. The required voltages for the set and reset states, although high, could be easily lowered by adjusting the thickness of the different layers of our material.

## I. INTRODUCTION

Information storage has always been an essential part of our culture, but it has become even more important as the Computer Age started. There is a whole industry producing massive data storage devices and researching for quicker access and higher capacities. Memristor devices are capable of storing bits of information by changing their resistance state. These types of memories are non-volatile and durable: the resistance value persists even if the device is disconnected from the power source. The device has two or more clearly distinct states, mainly a high resistance state (HRS) and a low resistance state (LRS), which in general are more than one order of magnitude apart from each other. These states can be exchanged with the application of an electrical potential in combination with an injection of carriers; and we can assign a logic state to each of them.

There are two types of resistive memories depending on how the change between these states is achieved. In unipolar switching, the current is only applied in one polarization, and the change of state is caused when the current reaches a critical value. In bipolar memories the potential must be inverted to modify the resistance state. The usual resistive random-access memory (RRAM) consists of an insulating material, with two metallic electrodes: one at the bottom and one at the top, in a metal-insulator-metal (MIM) structure This means that RRAMs only have two terminals, instead of the 3 typical terminals of CMOS devices (source, drain and gate), which allows the construction of smaller, more efficient structures [1]. This also means that, unlike flash memories, each bit can be accessed independently, increasing its data storage speed. Furthermore, all of the materials that are commonly used for the fabrication of memristors are fairly cheap, as well as environmentally friendly and relatively easy to produce, so they could become a perfect alternative to our current means of data storage. The main concerns of these devices are reliability, since memristors degrade with a relatively low number of cycles, and variability, as the transitions between states take place for different voltages.

The device we are working with is a bipolar memristor, and it is suggested that LRS is achieved by the formation of small conductive filaments (CF). [2]. For our device, the main mechanism involved in the forming of the CF is the valence change mechanism (VCM), as it is typical of metal oxides [3]. The process in which the CF are first created is called electroforming: the strong electrical field that is created as a positive voltage applied to the top electrode breaks the Si-O bonds, and the oxygen anions are transported up to the top electrode by the same field, where they are accumulated (either stored at the interface or absorbed by the top electrode). The CF consist in a series of silicon nanoinclusions, the nucleation of which increases in the presence of oxygen vacancies, until conductive pathways are formed [2]. The oxygen vacancies that are left may affect the valence state of the transition metals, which in turn may form a conductive path, which is responsible for the LRS [4, 5].

## II. DEVICE STRUCTURE AND PREPARATION

The studied device consists of a *p*-type Si wafer, on which a 2 nm $Si_3N_4$ layer is deposited, and then the wafer is provided with a $SiO_2$ layer with five rows of silicon nanocrystals with diamond cubic crystal structure, with possible deformations due to its reduced size [7]. In order to create this layer, alternating layers of $SiO_2$ (of 2 nm thickness) and SRON (Silicon rich oxynitride of 4.5 nm) were deposited and then put through an annealing process at 1150 °C in $N_2$ for 1 hour. Last, an additional 10 nm of $SiO_2$ were deposited on top. The deposition process was done by plasma-enhanced chemical vapor deposition (PECVD). To create the devices, a full area Al bottom contact was deposited on the back of the wafer; and ZnO contacts on top following a lithographic process. This anode is transparent to the visible range [5], so it allows us to perform electroluminescence experiments on the material, in which the material emits light when high currents circulate through the devices (although this phenomenon turned out to be quite insignificant for this specific device and was not the objective of this work). Nevertheless, ZnO is required as the defects that exists inside this type of anodes may absorb the oxygen anions produced during the forming of the CF, due to the intrinsic oxygen deficiency that this material presents. Also note that ZnO can act as a memristor, but not under the conditions of the deposition process employed [6].

Because of the substrate being *p*-type silicon, $Si_3N_4$ is used to improve the injection of minority carriers (electrons) thanks to its positive defects when positive voltages are applied during the set process, and it also serves as a buffer layer [8], increasing the durability and reliability. These insulators together with the layer of $SiO_2$ without nanocrystals provided certain thermal protection for the layer with nanocrystals during the annealing process.

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**TABLE I**: Thickness of the different components of our device. The materials are listed in the order they appear in the sample, from top to bottom.

| Material | Thickness |
|---|---|
| ZnO | 100 nm |
| $SiO_2$ (without nanocrystals) | 10 nm |
| $SiO_2$ (with nanocrystals) | 32.5 nm |
| $Si_3N_4$ | 2 nm |
| Si | Of the order of 1 μm |
| Al | 200 nm |

Note that $SiO_2$ is usually not a memristive material on its own, it requires the presence of oxygen defects to do so ($SiO_x$). A transition shell of $SiO_x$ is formed around these nanocrystals, the size of which depend on the temperature during the annealing process [7].

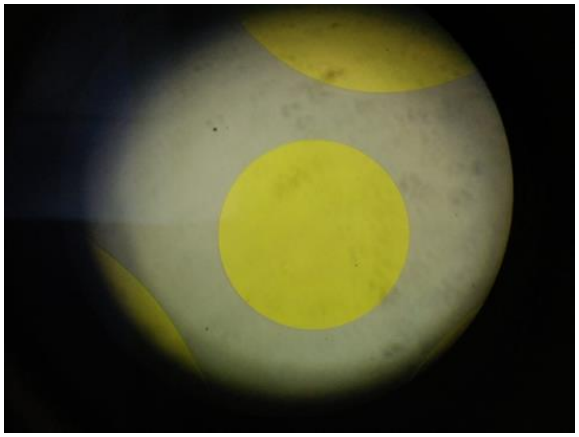

**FIG. 1**: Top view of a device on our wafer. The transparency of ZnO for visible light allows us to perform electroluminescence experiments. The sample was isolated during the measurements to avoid external interferences.

## III. MATERIAL CHARACTERIZATION

For electrical characterization we used a Cascade Microtech Summit 11000 probe station, consisting on a wafer chuck, a cylindrical piece where the material is fixed thanks to some small holes where vacuum is induced with an external pump, that also serves as an electrical contact to the ground. In order to prevent noise and external interferences, the laboratory where the measures were performed is insulated from its surroundings and the probe station forms a Faraday cage which cancels external fields. All of these preparations are crucial, as the currents we are expecting to measure can range from $10^{-12}$ to $10^{-3}$ A. The system allows small movements of the chuck, and also supports up to 4 micrometric needles from where the potential is connected to our waffle. A 20X power lens is used for assisting in selecting the desired device. The data was acquired using Agilent B1500A, a semiconductor device analyser with a resolution of tens of fA.

Two types of tests have been performed, applying voltages either by sweeping in a range or applying pulses. The first method is used for finding the voltages at which the CFs are formed and destroyed, while the second is used for testing reading and writing in the material in conditions similar to a real device operation. Our sweeping tests have been performed between 25 V and -20 V, with a step of 50 mV. The pulses consisted of the application of a $V_{set}$, a $V_{read}$ which was the same for both states and negative (the state is easier to identify at negative polarization), and a $V_{reset}$. The voltage and time of these pulses has been modified to try to improve the performance of our device. The system also lets us set a compliance current (CC), a maximum allowed value of the electrical current so our material does not break during the set process. The properties of the device vary greatly depending on this value, because of the limitation imposed to the CF formation [4]. Trying to detect these CF with transmission electron microscopy (TEM) is extremely difficult, as their formation is random, and their effective area can be four orders of magnitude smaller than the total device area.

## IV. EXPERIMENTAL RESULTS AND DISCUSSION

### A. Sweeping tests

Our devices have been tested performing 300 cycles, employing both no current compliance limitation and also 100 μA. For our material, intensities of the order of 1 mA were achieved during the set processes in devices with no compliance, thus the CC was chosen to be sufficiently different from this maximum, but also enough to be able to change the state of our memristor.

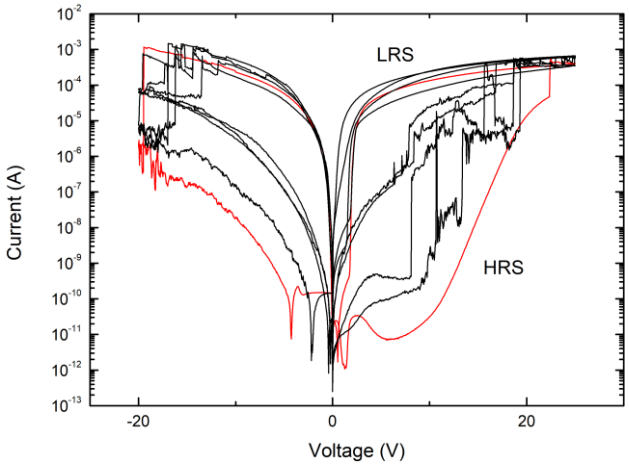


**FIG. 2**: First 5 cycles for our device, with no CC. The 1st cycle is presented in red, and typically requires the highest $V_{set}$. The current for this and all subsequent figures is presented as an absolute value, in logarithmic scale.

In the first part of the sweeping test, electroforming takes place and the CF are formed from the pristine state as the current though the device increases. During this process, partial dielectric breakdown of the material also takes place, as the device becomes more conductive with 2 or 3 cycles, as it can be seen in FIG. 2. This means electroforming is complete, and the two resistive states, HRS and LRS are now well defined.

When the voltage is increased during HRS, a sudden increase of the current intensity can be detected for a determined voltage value, $V_{set}$. This is the set process, where LRS is achieved as the CF are reformed by oxygen migration. The size of these CF depends on the current going through the device, and thus, the power consumption of the device may be adjusted by regulating the size of the CF [1]. During this

process, a limit to the maximum current can be applied to prevent permanent damage to the device.

During the reset process, an opposite tension is applied, and as current increases oxygen ions migrate from the top electrode back to their original positions, destroying the CF and increasing the resistivity of the material. This might be the cause why bipolar switching devices are usually more cyclable than the ones with unipolar switching [1]. In this process, the electrical fields and high temperatures play a crucial role, as the local Joule heating and the electrical field assists in the migration of oxygen vacancies and the reoxidation of the conductive filaments [2, 4]. It is for this reason that no limitation to the current is applied during reset operations. In a similar way to the set operation, a sudden drop in current takes place for a determined $V_{reset}$. The CF are destroyed, although not entirely: only the region closer to the top electrode. This can be seen in the required set voltages, as the firsts cycles tend to require a higher potential for the electroforming of the CF that the following cycles for achieving HRS.

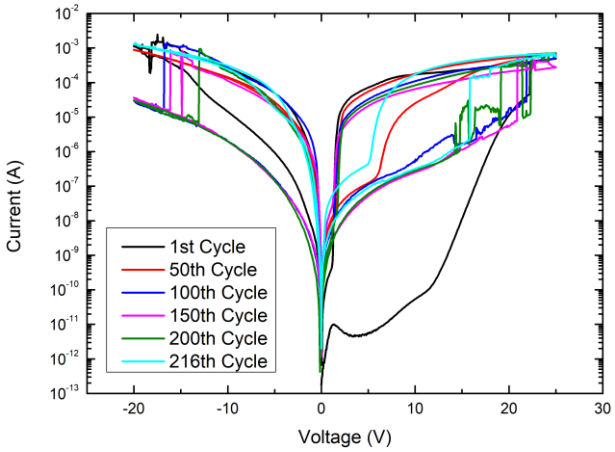


**FIG. 3**: Cycles performed on our device, without using any CC. The first curve corresponds to the pristine state, were the device has not been modified and thus the conductivity is very low. Even if the set process is not correctly performed during the 50th cycle, the device continued performing set and reset operations correctly for up to 216 cycles.

For the test with no CC, the set process was correctly performed for 216 cycles. FIG. 3 show how the HRS of the material becomes more conductive as it performs more cycles, and it can be seen how for the 216th cycle, in the LRS state the current rapidly falls for lower voltages and the reset is missing: the device is broken. However, the resistance ratio between the two states is at least of 2 orders of magnitude for up to 200 cycles. The results of the test with CC are shown in FIG. 4. For the same number of cycles, the difference between both states is about an order of magnitude bigger than when we used no CC. The HRS remains very resistant even when the device breaks, improving the overall sensitivity.

TABLE II shows the voltages for which most of the set and reset processes happen and the number of cycles performed before the device broke. There was no correlation found between the number of cycles and $V_{set}$ or $V_{reset}$, although there is some tendency for cycles with higher $V_{set}$ to also require higher $V_{reset}$ for the device to return to the HRS. This can be explained by the formation of multiple conduction paths or their increase in size. Although it may seem surprising that the number of cycles is similar in both cases, in FIGS. 3 and 4 can be clearly seen how the use of compliance prevents conductivity from increasing with each cycle, thus protecting the device from damage. We can also see that lower $V_{reset}$ values are required when CC is applied. This makes sense, as the use of CC limits the formation and size of the CF, and thus the device is easier to reset. TABLE III presents the resistance values for some of the cycles. The first cycle is really resistive, since electroforming is taking place. We see that with more cycles, the gap between the two resistance states decreases. The LRS tends to become less conductive. The HRS should become more conductive, although the resistance values also depend on how the reset process was performed.

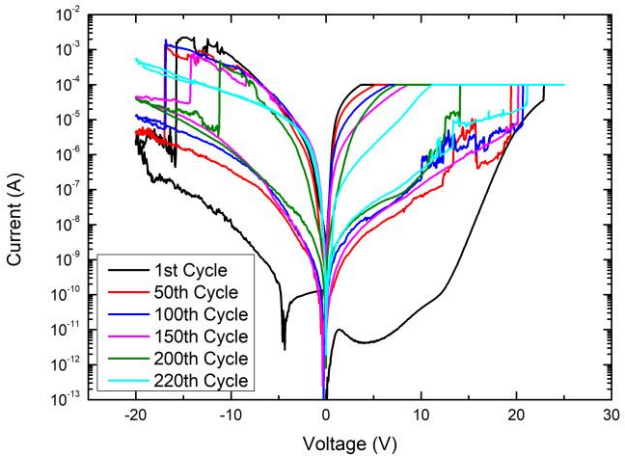


**FIG. 4**: Cycles performed on our device, limiting the maximum current through the device to 100 µA during the set process. Up to 220 cycles were performed successfully.

**TABLE II**: The voltages shown in this table are not the only ones found experimentally, but they were the most common. While the upper bounds are quite stable, the lower bounds may be up to 6V lower than the values shown in the table.

| CC | $V_{set}$ (V) | $V_{reset}$ (V) | Cycles |
|---|---|---|---|
| No | 17 - 23 | 14 - 20 | 216 |
| 100 µA | 17.8 – 21.7 | 12 - 17.5 | 220 |

**TABLE III**: Values of the resistance at V = 3V, for 5 different cycles, both with and without compliance.

| | $R_{HRS}$ (Ω) | | $R_{LRS}$ (Ω) | |
|---|---|---|---|---|
| **Cycle** | **No CC** | **CC = 100 µA** | **No CC** | **CC = 100 µA** |
| **1st** | $6.5\cdot10^{11}$ | $5.9\cdot10^{11}$ | $8.7\cdot10^{4}$ | $4.1\cdot10^{4}$ |
| **50th** | $5.2\cdot10^{7}$ | $1.2\cdot10^{9}$ | $1.3\cdot10^{5}$ | $7.3\cdot10^{4}$ |
| **100th** | $7.2\cdot10^{7}$ | $3.6\cdot10^{8}$ | $2.3\cdot10^{5}$ | $1.6\cdot10^{5}$ |
| **150th** | $1.9\cdot10^{8}$ | $6.4\cdot10^{8}$ | $2.9\cdot10^{5}$ | $5.3\cdot10^{5}$ |
| **200th** | $1.6\cdot10^{8}$ | $2.2\cdot10^{8}$ | $2.5\cdot10^{7}$ | $6.1\cdot10^{5}$ |

Our device also showed signs of a different resistance state between HRS and LRS, as can be seen in the last two curves of FIG. 2, which tended to appear around $V_{set}$ = 8-11V. However, all attempts to access to this state without reaching to LRS resulted in failure, probably due to this state being not stable, contrary to the LRS previously described. This state does not appear when using CC, so seems that is high dependant on the set process, and this would explain why it is unstable if tried to reach on its own.

### B. Pulse tests

Two pulses tests have been performed on different devices. Prior to each of the tests, three voltage sweep cycles between 25V and -20V were performed in each device, with or without CC. Afterwards, pulses were applied following the pattern shown in FIG. 5.

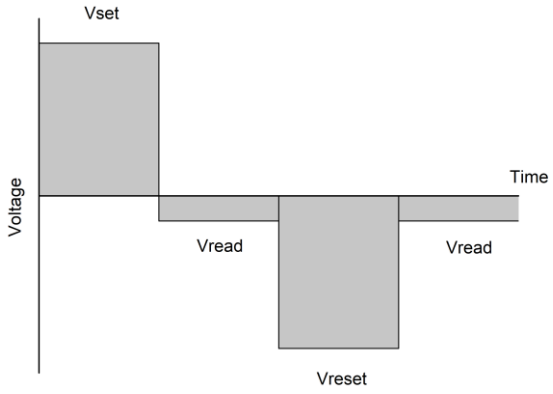


**FIG. 5**: Sequence of pulses that conform a cycle. Note that the pulses used for reading are both negative. This is due to the difference between the two resistance states being greater for negative voltages (accumulation conditions).

The pulses had the same current limitation as the one used for the electroforming sweeps in each case. We also could change the duration of each pulse, as the change of state not only depends on the voltage but also on the time it is applied. TABLE IV shows the parameters used for the study without compliance, set and reset voltages were chosen within the ranges shown in TABLE II.

**TABLE IV**: Parameters used for the study without compliance. Note that the duration of the reset pulse is higher, as it usually requires higher current.

| $V_{set}$ (V) | $V_{reset}$ (V) | $V_{read}$ (V) | $t_{read}$ (s) | $t_{set}$ (s) | $t_{reset}$ (s) |
|---|---|---|---|---|---|
| 20 | -20 | -2 | 0.0001 | 0.05 | 0.5 |

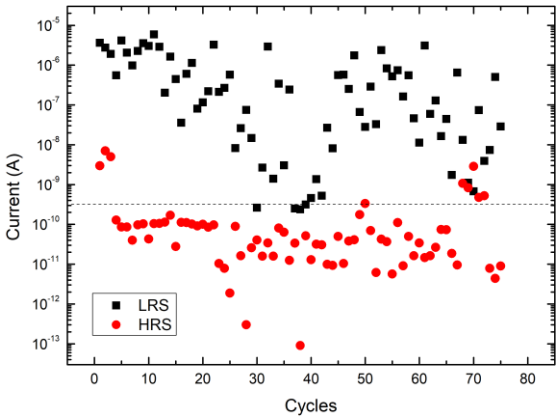


**FIG. 6**: Pulse test performed without CC. 75 readings are shown. If we consider the stripped line as our criteria for distinguishing both states, the device failed 13 times, a 17.3% of the total.

As can be seen in FIG. 6, the device clearly shows two different states. Although some values of intensity for LRS could be mistaken for a LRS in some cycles, please note that in most of these cases the difference between both states in a same cycle is of the order of at least half order of magnitude.

**TABLE V**: Starting parameters for the pulse test with CC = 100 μA. At 400 and 600 cycles, $t_{set}$ was doubled to try to improve the resistance ratio between the LRS and HRS.

| $V_{set}$ (V) | $V_{reset}$ (V) | $V_{read}$ (V) | $t_{read}$ (s) | $t_{set}$ (s) | $t_{reset}$ (s) |
|---|---|---|---|---|---|
| 20 | -20 | -3.3 | 0.0001 | 0.05 | 0.2 |

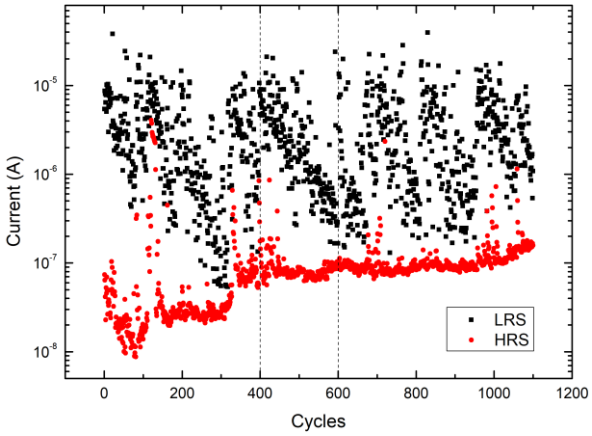


**FIG. 7**: Pulse test performed with a maximum current of 100 μA. 1100 cycles are shown. Each stripped line represents one of the changes to $t_{set}$, which was doubled each time, as we were trying to improve the resistance ratio between the two states.

The starting parameters for the test with compliance appear at TABLE V. A lower $t_{reset}$ was chosen this time, to try to make the set process easier. Two states are clearly shown in FIG. 7. The HRS was very stable, but as cycles were performed the conductivity of LRS was decreasing, which we tried to correct by doubling the duration of the set pulse. Note that the first change at 400 cycles was especially effective in this regard, as the difference between both states greatly increased, but with enough cycles this ratio began to decrease again. We can also see how the HRS becomes more conductive the more cycles are performed.

### C. Retention tests

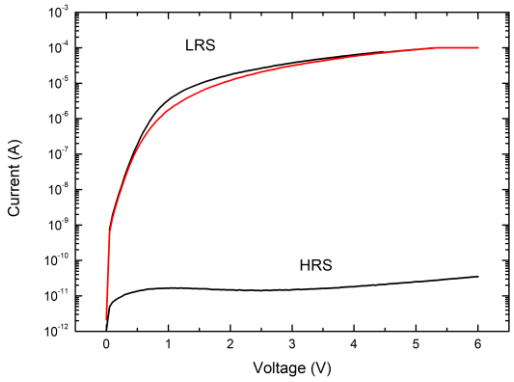


**FIG. 8**: Retention test performed with CC, on a device with two cycles. The state was read 2 hours after the last cycle was performed. The black curves belong to the last reset operation performed, and the red curve was measured after two days since the set process. The current was measured for up to 6V.

Two retention tests have been performed in our material. Devices have been set to the LRS state both with and without CC, and then the state has been read after 2 hours, and then after 2 days. Both retention tests have been performed on devices with a low number of cycles: 2 cycles for the 2 hours test and 21 cycles for the 2 days test. FIG. 8 shows how the state was retained almost perfectly, with a maximum difference in current of the order of a few μA. FIG. 9 shows how after two days, however, the resistance value of LRS increased about an order of magnitude. Tests for larger intervals of time have yet to be performed.

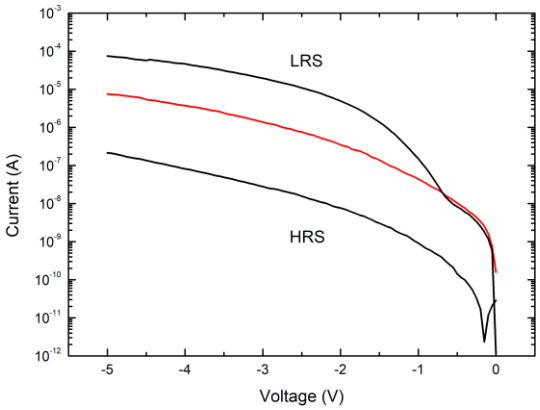


**FIG. 9**: Retention test performed on our device. LRS state was achieved without CC, and the current was measured for up to -5V.

## V. CONCLUSIONS

In this paper, a device made of $SiO_2$ with alternating layers of Si nanocrystals has been studied and it has been found to behave as a memristor. The fact that this material becomes a memristor when supplied with Si nanocrystals is worth studying and gives birth to some choices of fabrication that could lead to a better performance of the material. Although its characteristics are still far from the ones we could consider desirable for a commercial memristor, its cyclability has proved to be not outstanding, but above the average for this kind of devices. The fact that the LRS is still retained after 2 days is proof of the device stability. Also, the appliance of a CC is a key factor to improve the cyclability and sensibility of the device, especially when working with pulses. Some of the characteristics of our device can still be improved, for example the required voltages for the set and reset processes could be lowered by reducing the thickness of the material. This could also imply shorter pulses, which would in turn increase the performance of our device.

A third state of resistance has been found and, if stabilized, it could be used for working with lower voltages without the need of a current regulator (or even using a lower current limit to improve the cyclability of the material), or for neuromorphic applications. This way, three memory states become accessible within one same device, and they could be reached with only two terminals, by applying pulses with higher voltages, longer durations, or even by applying two pulses when the terminal is at the middle resistance state.


### Acknowledgments

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