Chapter 10

Bioelectronics for Amperometric Biosensors

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Additional information is available at the end of the chapter

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1. Introduction

The Discrete-to-Integrated Electronics group (D2In), at the University of Barcelona, in partnership with the Bioelectronics and Nanobioengineering Group (SICBIO), is researching Smart Self-Powered Bio-Electronic Systems. Our interest is focused on the development of custom built electronic solutions for bio-electronics applications, from discrete devices to Application-specific integrated circuit (ASIC) solutions.

The integration of medical and electronic technologies allows the development of biomedical devices able to diagnose and/or treat pathologies by detecting and/or monitoring pathogens, multiple ions, PH changes, and so on. Currently this integration enables advances in various areas such as microelectronics, microfluidics, microsensors and bio-compatible materials which open the door to developing human body Lab-on-a-Chip implantable devices, Point-of-Care in vitro devices, etc.

In this chapter the main attention is focused on the design of instrumentation related to amperometrics biosensor: biopotentiostat amplifiers and lock-in amplifiers. A potentiostat is a useful tool in many fields of investigation and industry performing electrochemical trials [1], so the quantity and variety of them is very extensive. Since they can be used in studies and targets as different as the study of chemical metal conversions [2] or carcinogenic cells detection, neuronal activity detection or Deoxyribonucleic acid (DNA) recognition, their characteristics are very varied.

For chemical measurement systems in biological applications, potentiostat amplifiers [3] are the electronic interface to a large category of amperometric chemical sensors which are capable of managing many biologically and environmentally important analyses. This characteristic gives us the possibility of building an extremely versatile tool with other interesting specs: portability, accuracy and reliability.

Demand for increased functionality, smaller systems, with smaller electrodes, for ultra-low current detection and versatility will force potentiostat amplifiers to be designed on a system-on-chip (SoC), combining single to multi-sensor measurements, to be implemented in advanced Complementary metal–oxide–semiconductor (CMOS) processes. The scaled supply voltages in these processes [4-8], however, seriously limit the chemical analysis range.

Interesting approaches have been designed in terms of the instrumentation [9-13], attempting to work with low-voltages and low-currents, these electronics are integrated with autonomous powering. In [10] the authors propose an interesting low-power concept of a two-electrodes approach with the capability to measure from 1pA to 200nA with a simple Analog-to-Digital (ADC) approach, but operating at 5V. [11] presents a nice approach based on a Sigma-Delta modulator with the capability to check currents with a sensitivity of 50fA with a power dissipation of 12 μW, operating at 3.3V in this case, but with all the processing electronics being external to the prototype. In [12] a Complementary metal–oxide–semiconductor (CMOS) approach is presented for electrochemical arrays, operating with a bias of 5V, where the array (5X5) is placed in the same substrate with the amperometric detector. The design works in an unipolar fashion detecting pA, with a maximum operating frequency @ 2kHz. Good approach is also presented in [13] where a current-mirror circuit is implemented for three-electrode amperometric electrochemical sensors. There the system has an accuracy of 1%, with a range of currents of 1nA to1μA, operating at 1.8V with a power consumption of70μW. [14] present a 5V, 0.6mA amperometric electrochemical microsystem array (4X4), with a range between 6pA to10μA, where full electronics and array are placed on-chip, also working with an unipolar approach, with a chip size of 2.3X2.2 mm, with the electrode array implemented with electrodes of 2mm of diameter. Also in [15] a similar approach is derived, with an array of 8X8, with circular electrodes of 6μm, and a second implementation with the array implemented in-chip with the electronics. First Cyclic voltammetry (CV) approaches are presented with a typical range between 0.1V to 0.8V, detection currents from-1.5μA to 1.5μA.

Latest advances have been reported in [16] and in [17]. In [16], the novelty resides in the technological approach for the electronics design. Generally, all the implementations are based on silicon electronics, looking for a cheapest massive production and good properties. In this case Poly-Si Thin-Film transistors are used, ideal for their flexibility. In this particular work the system it is just conceived for a single three-based electrode for a cyclic voltammetry to detect diabetes. Electronic performances are not significantly inferior to those based on a CMOS solution. The system operates at 1.2V, working between 0.111V to 0.679V, but not reference is addressed to the power consumption and current range. The last example [17] is quite interesting and a great approach to our concept, but also is an excellent example of the challenge of the present proposal. This system has the capability to define different stimulus for the amperometric and electrochemical measurement. It provides linear sweep, constant potential, cyclic and pulse voltammetry, with enough smart facilities, but the system presents a fixed clock and a maximum power dissipation of 22.5mW, for an array of just 2X2 electrodes. The budget of 22.5mW is a lot of power for the present concept. As a readout circuit, it has good performances, between±47μA, with a linear resolution of 0.5pA.

In terms of the Lock-In Amplifiers, the measurement must be processed in order to extract the impedance variation of the cell. In an electrochemical cell, electrode kinetics, redox reactions, diffusion phenomena and molecular interactions at the electrode surface can be considered analogous to the above components that impede the flow of electrons in an ac circuit. The simplest electrical modelization is based on an equivalent RC circuit, also called a Randles circuit.

In order to proceed with the signal processing there are two main approaches: a) the Fast Fourier Transform (FFT) [18], and b) the Frequency Response Analyzer (FRA) [19]. In the case of the FFT, a pulse, or a step, -the approach to be followed is the ideal Dirac function-, is applied to the sample because it contains a wide frequency content. Then, the response of the sample is digitized and processed in a digital processor, for instance a DSP (Digital Signal Processor), and using the FFT algorithm, the different frequency components are obtained for their analysis. Another possibility is the logarithmic sampling in the DFFT calculus, reducing the data required in the process.

A simpler solution is based on the FRA approach. In this case a sine and cosine signals are adopted and using two multipliers and a filter stage the real and imaginary components of the response are obtained. This measurement must be done for each frequency. Working with just one sensor and in terms of the size of the final product, the FFT option could be adopted, because the response for several frequencies is obtained. The FRA solution is a solution more oriented to multi-sensor approaches but also in the case of single sensors it is also a good option, in terms of the trade-off between complexity and speed, if not too low frequencies are to be measured. This lock-in approach is more feasible.

The perturbation signal provided by the instrumentation system – following the FRA approach – generally uses a sinus wave as the input voltage.

The chapter would present the state-of-the art in the conception of the involved electronics for the potentiostat amplifier instrumentation and EIS approaches, analogue and digital.

2. Amperometric biosensors

Nowadays advances in different multidisciplinary areas like microelectronics, microfluidics, microsensors and bio-compatible materials open the door to developing advanced biomedical solutions for health care, such as Point-of-care devices, combining Lab-on-a-Chip solutions with suitable electronics for measurement, processing and remote telemetry communication [20-22].

In particular, integration of medical and electronic technologies allows biomedical devices solutions capable of diagnosing and/or treating pathologies by detecting and/or monitoring pathogens. There are different approaches for amperometric biosensors instrumentation, based on a potentiostat amplifier with several different amperometric readout configurations [13,23,24].

The interest in electrochemical sensors, and in particular amperometric biosensors, started when changes in the dielectric properties of an electrode surface were detected by potentiostatic methods [1,25,26]. These biosensors are capable of detecting antigens, antibodies, proteins, DNA fragments, PH changes, heavy metal ions, and so on [27-31].

There are different solutions for the electrochemical-based instrumentation that vary from discrete to mixed and full custom-ASICs approaches. The sensor size and the system complexity define the final adopted solution. Electronic designs based on low-cost on the shelf surface mount components can be adopted for electrodes areas greater than 1 mm^2. Full custom ASIC solutions are valid approaches [8,30,31] for smaller and multiplexed sensors. Moreover, these ASIC solutions are indicated if very low current levels are derived from the sensors. Other key indicators for an ASIC solution near the electrodes are not only the degree of miniaturization, but also the fact that EMI (Electromagnetic Interference), can be reduced, and external disturbances such as vibrations, moisture, sources of electrical noise, etc. are avoided.

The development of multisensory arrays of biosensors, working with low concentration levels and the capability of a multi-bio-analysis in blood (searching for a multi-pathogen detection), is a topic of great importance in the contemporary situation [32,33].

2.1. Electrochemistry and reactions on the electrode

Electrochemical biosensors are the largest group of chemical sensors. These biosensors are normally based on enzymatic catalysis of a reaction that produces or consumes electrons (such enzymes are correctly called redox enzymes). Electrochemical sensors allow three main configurations: voltammetric, potentiometric and conductometric measurements [3]. In the present chapter special interest is focused on the voltammetric sensors. Voltammetric biosensors are those based on the measurement of the current-voltage variations. Amperometric biosensors are a particular case, where determined electrical currents are associated with a redox process where a fixed voltage in the sensor is applied. Some associated current, called faradaic current, is exclusively generated by the reduction or oxidation of some chemical substance at an electrode [34].

Under equilibrium, and in the absence of an externally applied voltage, a polarizable electrode resting in solution will develop a potential based on the ratio of the solution's chemical species [1]. When voltage is applied to the electrode the system is forced out of equilibrium and results in a reduction/oxidation (redox) reaction:

$$O + ne^- <=> R \tag{1}$$

where O is the oxidized form of the species, n is the number of electrons per molecule oxidized or reduced, e- is an electron, and R is the reduced form of the species. This results in a faradic current at the electrode surface for reversible systems also called Nernstian systems [1].

2.2. Electrochemical cell

Typical amperometric sensors configuration is based on two or three electrodes cell topology. A typical two electrodes topology is defined by the working electrode, where the electrochemical reaction takes place and the reference electrode, in addition to the auxiliar electrode which tracks the solution potential and supplies the current required for the reaction. This topology brings some kind of problematic behavior by the auxiliar electrode polarization effects. While the auxiliar electrode is assumed to have a fixed well-known potential some charges are accumulated on the electrode, due to the current supply, making this assumption erroneous. In order to avoid this effect, we need to supply the current using an extra electrode. The three electrodes configuration, which is defined as follows: a) the working electrode (WE), surface where the electrochemical reaction takes place; b) the reference electrode (RE), which tracks the potential solution and c) the counter or auxiliar electrode (CE), which supplies the current required for the electrochemical reaction at WE, is then of special interest.

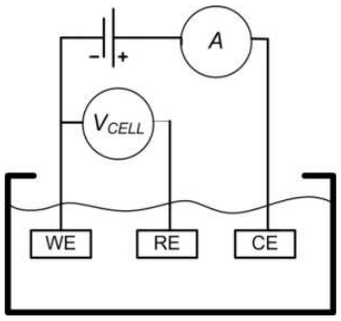

Figure 1. Three electrodes sensor topology.

$$V_{WE} - V_{RE} = V_{CELL} \tag{2}$$

We must consider the potential solution V_{CELL} voltage to be constant, so in order to keep this condition current through the RE electrode should ideally be zero, avoiding any electrode polarization effect. The current supply is provided by CE, avoiding this undesirable effect.

So, considering the three electrodes topology, once any polarization effect has been avoided, one of the key points to be studied is the theoretical model in terms of the electronic behavior of the electrochemical cell.

An electrochemical sensor must be considered, in an electrical model, as an impedance [28,35], taking as a basic sensor element the presence of a capacitor, used to describe the interface between the electrode and their surrounding electrolyte. This capacitance is based on the electrical double-layer theory [36], so electrodes immersed in an electrolyte solution, can be described as a capacitor storing charge (ions from a solution absorbed on the electrode surfaces).

We must consider this interface model as an electronic representation in terms of electronic passive elements, and it can be very complex. The simplest case uses an equivalent circuit, also

called a Randles circuit [1], depicted in Figure 2, which is formed by the double-layer capacitor (Cref), in parallel with a polarization resistor (Rref), which is also described as a charge transfer resistor, and the solution resistor (Raux). This is the electrical model that can be adopted for a mathematical description. Such description is very useful to create an electrical model for the electrochemical cell theoretical impedance analysis, being easy to reproduce in different electronic software emulators or prototype testing, capable of representing the electrochemical cell by means of passive elements like resistors and capacitors. This model can evolve into a more complex one, bringing us the possibility of an easier sensor functionalization, instrumentation design and prototype developing and testing [37].

The impedance measured in the cell is defined by (3), being Z_{CELL} the relation $V_{CELL}(t)/I_{CELL}(t)$.

$$Z_{ref\text{-}work}(j\omega) = Z_{CELL}(j\omega) = \frac{R_{ref}}{1 + j\omega R_{ref} C_{ref}} \tag{3}$$

One of the most interesting features that can be easily achieved with a three electrodes topology is the possibility of developing a multi-bio-analysis system by means of different electrode arrays. These arrays can be used as a multi-purpose system becoming an extremely versatile tool making it feasible to perform at the same time different electrochemical experiences with different biochemical species, average measurements through time or area, etc. [8,38,39].

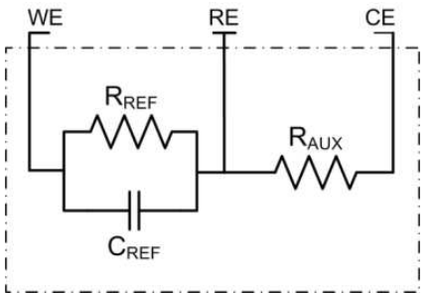

Figure 2. Randles Model for electrochemical cells.

3. Electronics for amperometric biosensors

3.1. The potentiostat amplifier

A potentiostat amplifier is a useful tool in many fields of investigation and industry performing electrochemical measurements [1], so the quantity and variety of them are very extensive, having different characteristics. In this section, we will focus our attention on the development of an analogue potentiostat amplifier approach.

Two different approaches can be followed in the design and implementation of a potentiostat amplifier: a discrete or integrated solution. In order to design a portable system for standard electrochemical assays, a discrete implementation is an extremely good solution in terms of

portability, accuracy and economy being a standard on electrochemical experiments. But demand for increased functionality, reduced system size, reduced size of the electrodes, defining complex arrays of sensors, ultra-low current detection and versatility, are introducing a major interest in system-on-chip (SoC) solutions, to be implemented in advanced CMOS processes. The scaled supply voltages in these processes [4-8], however, seriously limit the chemical analysis range.

Driving voltages of amperometric chemical sensors do not scale with electrode size, but are instead defined by the reduction/oxidation (redox) potentials of the analyses being investigated, as stated in [40] many analysis are undetectable using standard potentiostats in a 0.18μm CMOS process due to its maximum supply voltage of 1.8V.

The main tasks of these kind of structures (Figure 3.) are the measurement and recognition of some kind of particles in a media (or the media itself), through the application of an electric signal and the readout and conditioning of an output signal.

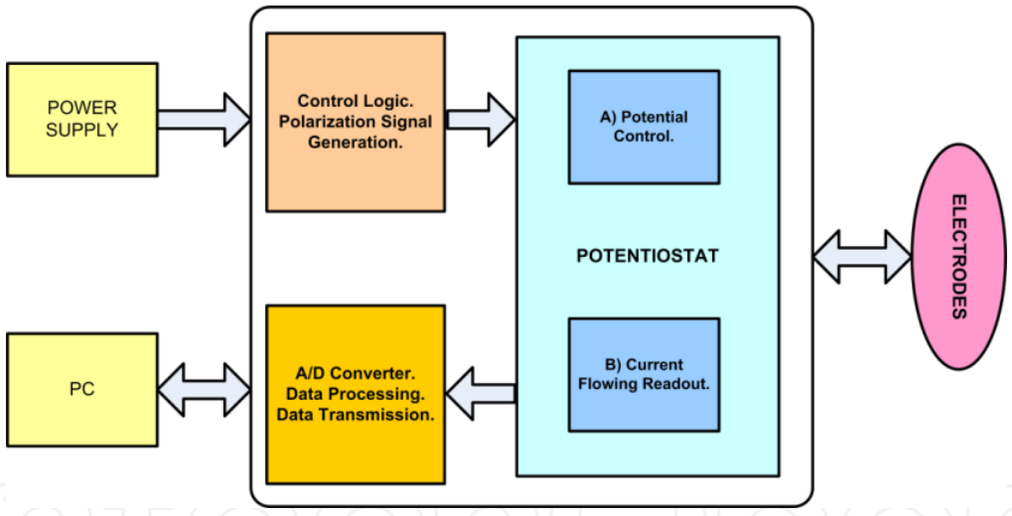

Figure 3. Potentiostat general scheme.

The main functionalities envisaged for a potentiostat amplifier are: a) driving the sensor electrodes with the desired signal V_{CELL}, ensuring that this voltage remains invariable and supplies the current necessary for the electrochemical reaction, potential control module on Figure 3. (section 3.1.1), and b) be able to extract an output signal which is the measuring of the current flowing through the electrochemical cell, current measurement module on Figure 3. (section 3.1.2). Driving the electrochemical cell depends on whether the configuration is based on two or three-electrodes, as stated above. Different approaches are conceived to fulfill this last objective.

3.1.1. Potential control configurations

As has been stated before, one of the main tasks of a potentiostat is the control of voltage difference between working and reference electrodes of the electrochemical cell and supplying the required current from or into the electrochemical cell through the counter electrode.

This task can be realized with two different circuit configurations, grounded working electrode and grounded counter electrode, the first being the most popular configuration depicted in Figure 4 which illustrates the basic implementation of this configuration. As shown, the working electrode is kept at the ground potential and an operational amplifier, called the driving amplifier, controls the cell current I_{CELL}, so the cell potential V_{CELL} is at the desired potential V_{IN}.

The system operation is very simple, but, like other electronic instrumentation circuits, we get potentiostat functionality limitations due to its own driving amplifier limitations. Since current flow in the reference electrode changes the potential of the reference electrode due to polarization effects (see section 2.2), driving amplifier input bias current should be small and input resistance should be very large. Depending on the target, you must consider several limitations on the driving amplifier parameters. Voltage gain and input offset voltage of the driving amplifier define the accuracy and linearity of the potential control. Other important parameters to be considered are the output voltage swing, input referred noise, bandwidth and slew rate, considering the stability as a sensitive issue due to the fact that the electrochemical cell is the load and feedback network of the amplifier.

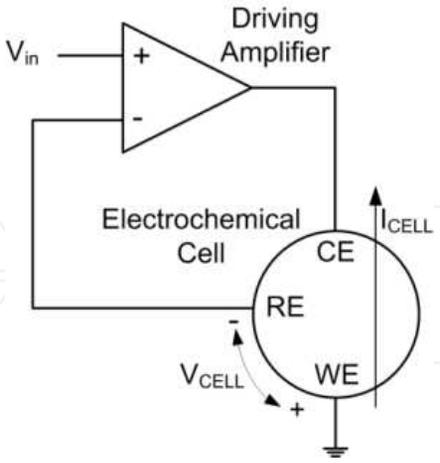

Figure 4. Potential control. General scheme.

In section 2.2. a typical electrochemical cell model has been depicted, where frequency dependent impedances like capacitors are present, the frequency and transient simulations of these impedances being quite complex to study. For this reason, it is necessary that the

potentiostat provides stability over wide operation ranges, being able to carry out diverse electrochemical experiences for different biochemical species.

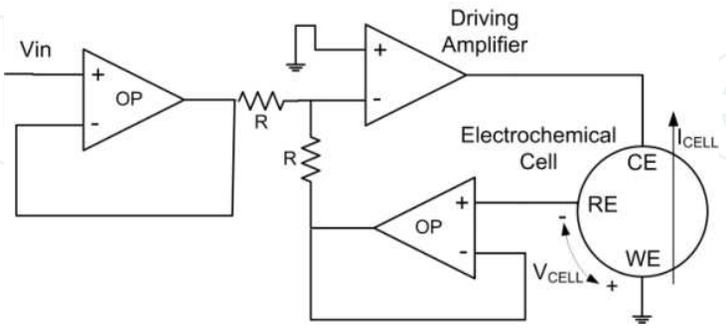

Figure 5. Using voltage buffers to isolate driving amplifier and reference electrode.

3.1.2. Current readout configurations

Some circuits used to fix the electrochemical cell's driving signal have been reported. The next stage concerns circuits related to the flowing current readout. Different approaches can be adopted and are presented in this section.

3.1.2.1. Transimpedance amplifier stage

In the present configuration the measurement is based on the direct conversion of the current generated in the electrochemical cell into a voltage signal using a transimpedance configuration, depicted in Figure 6 dotted rectangle.

In order to read the faradic current generated by the reaction I_{CELL}, a transimpedance ance stage amplifier (TIA), converts it to a voltage signal by means of a single resistor, as is indicated in (4), so the output signal $V_{out,TR}$ is equivalent to the faradic current through working electrode.

$$V_{out,TR} = - I_{CELL} \cdot R_{TIA} \tag{4}$$

The system operation it is simple, but, as is stated in the previous section, we get functionality limitations due to transimpedance amplifier limitations. V_{IN} voltage will be tracked to the electrodes if WE electrode is ground referenced, assuming operational amplifier virtual ground. In that case, input offset voltage and input referred noise must be considered in order to provide a steady virtual ground. Since generated current must flow through trans-impedance amplifier resistor R_{TIA}, trans-impedance amplifier TIA input bias current should be small and input impedance should be very large in order to minimize any current losses through this stage.

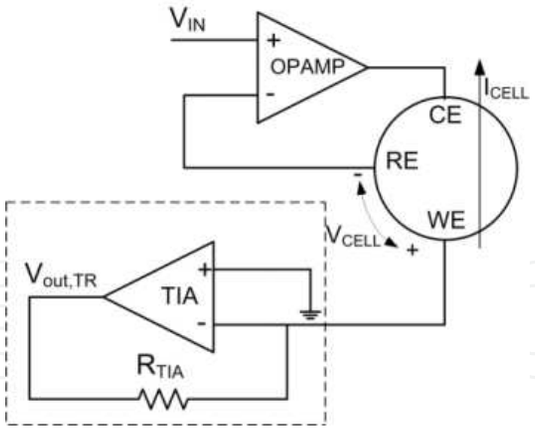

Figure 6. Basic grounded working electrode driving control configuration with a transimpedance amplifier readout stage.

As is shown on the operational amplifier equivalent circuit in Figure 7, the input impedance is the equivalent impedance between the positive and negative inputs. This impedance is linked to some leakage currents (I_{offset}), which could cause problems both in I_{CELL} current readout and V_{CELL} tracking, especially when extremely low faradic currents are generated on the reaction in which case a very high transimpedance resistor is required. This error in both cases can be minimized by reducing amplifier offset and bias current by means of very high input impedance.

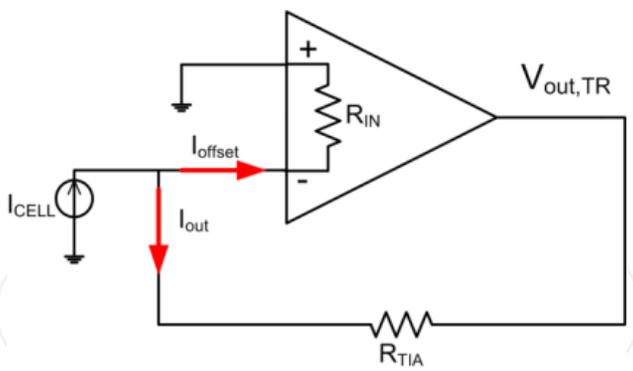

Figure 7. Operational amplifier in transimpedance configuration. General Scheme.

Other parameters to be considered are the amplifier's flicker and thermal noise or inherent current and voltage offset. Flicker and thermal noise are inherent to electronics and are characterized as an output voltage (Vnoise) (5) or as an input current (6) defining the transimpedance amplifier stage resolution, establishing a minimum signal to noise ratio, SNR (7).

$$V_{OUT} = V_{out,TR} + V_{noise} \tag{5}$$

$$I_{noise} = \frac{V_{noise}}{R_{TIA}} \tag{6}$$

$$SNR = \frac{I_{CELL}}{I_{noise}} \tag{7}$$

There are different solutions to maximize resolution of the measurement, increasing the SNR (Signal-to-noise ratio), and sensitivity, reducing thermal and flicker noise. For instance, one of the best solutions is based on chopper modulation, which implies more complexity on the design. A simplest solution is to just place a bandwidth filter. The capacitor on transimpedance amplifier feedback loop should remove the inherent 50 Hz network or any other frequency noise and harmonics but does not permit to avoid flicker noise problems. Figure 8. Depending on the application, if the system is required to work in a limited range of frequencies, like amperometric and voltametric experiences where you apply DC signals, or potential sweeps with an scan-rate of less than 1000 mV/s [1], it is useful to filter low frequencies to remove network powering noise, typically 50Hz and harmonics, and reduce thermal and flicker spectra to improve the SNR.

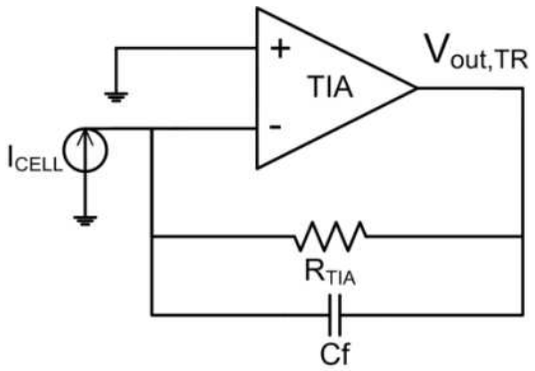

Figure 8. Transimpedance amplifier stage. Low-pass noise reduction capacitor configuration.

3.1.2.2. Instrumentation amplifier stage

This kind of current measurement topology consists in the direct conversion of the current in to a voltage signal by means of a resistor on the counter electrode, and an instrumentation amplifier that measures the voltage difference in the resistance, Figure 9.

We assume that the current through resistor R, is equal to the faradic current developed by the electrochemical reaction (I_{CELL}), and it is considered that voltage between reference and working electrode (V_{CELL}) is more steady than in the transimpedance amplifier stage due to the direct connection of working electrode to ground.

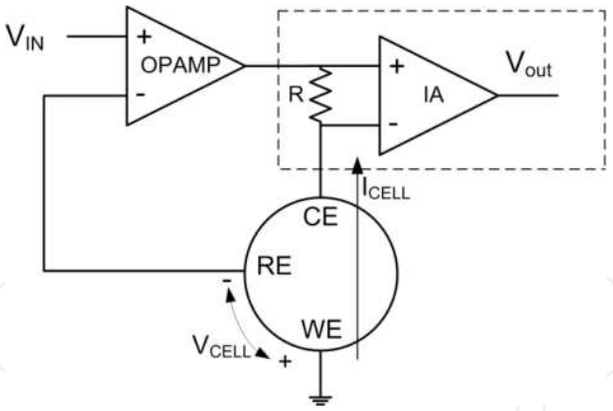

Figure 9. Basic grounded working electrode driving control configuration with a instrumentation amplifier readout stage.

An instrumentation amplifier transfer function is theoretically described by this equation:

$$V_{OUT} = A \cdot (V_+ - V_-) \tag{8}$$

Where A is the amplifier's gain and (V+ - V-) is the voltage difference on the amplifier's positive and negative, so we can determine that if the voltage (V+ - V-) is (9) the output signal is equivalent to the faradaic current through working electrode (10).

$$(V_+ - V_-) = I_{CELL} \cdot R \tag{9}$$

$$V_{OUT} = A \cdot I_{CELL} \cdot R \tag{10}$$

There are some parameters to be considered as a source of noise errors:

Input impedance.

Offset current, bias current.

Amplifiers are a source of noise and non-idealities that are critical, mainly if very low current resolution, such as nanoamperes or picoamperes is desirable. It will be assumed that all the amplifiers have an input bias current that interferes with the current readout system. In order to minimize these effects we need to use an amplifier with very high input impedance, as is depicted in the previous section. There are other parameters to be considered, such as resistor tolerance and resistor thermal noise. This stage is very dependent on resistors, the conversion of the flowing current to a measurable output voltage it depends on the stability of three different resistors. There is a very high probability of getting an error source, making impossible to get a very precise measurement, if the system depends on the tolerance and thermal noise of three different resistors, but it's possible to minimize output voltage dependence of this large number of resistors (Figure 10.).

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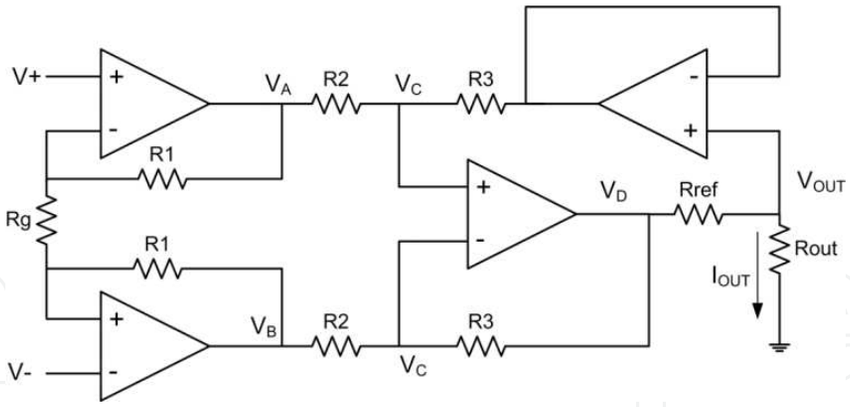

Figure 10. Modified instrumentation amplifier.

The modified instrumentation amplifier transfer function is theoretically described by the following equations:

$$\frac{(V_A - V_-)}{R1} = \frac{(V_- - V_+)}{Rg} = \frac{(V_+ - V_B)}{R1} \tag{11}$$

$$\frac{(V_B - V_C)}{R2} = \frac{(V_C - V_{OUT})}{R3} \tag{12}$$

$$\frac{(V_A - V_C)}{R2} = \frac{(V_C - V_D)}{R3} \tag{13}$$

Combining these three equations and considering that R3 = R2

$$V_{OUT} = I_{OUT} \cdot R_{OUT} \tag{14}$$

$$(V_{OUT} - V_D) = (V_A - V_B) = (V_+ - V_-)\left(1 + \frac{2R1}{Rg}\right) = I_{OUT} \cdot Rref \tag{15}$$

And if we consider

$$Rref = R_{OUT}\left(1 + \frac{2R1}{Rg}\right) \tag{16}$$

$$I_{OUT} = \frac{(V_+ - V_-)}{R_{OUT}} \tag{17}$$

We found that the output current signal is the same current as through electrodes and the evaluation only depends on the value of one resistor.

Regarding other error sources, the fact that there are no active components in the flowing current path, and being both flowing current and measured voltage referenced directly to ground, gives the system better stability than in the transimpedance amplifier stage.

3.1.2.3. Switching capacitors solution

Another feasible solution to current readout is the switching capacitors transimpedance stage avoiding the use of resistors. This topology needs a clock control signal, but, assuming the possibility of using a microcontroller for a later signal processing or data transmission this should not be a problem. The basic circuit approach is depicted in Figure 11.

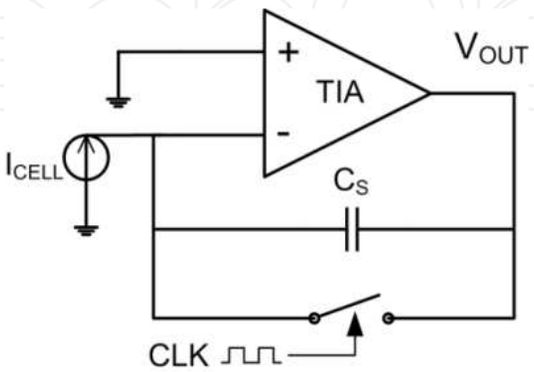

Figure 11. Switching capacitors transimpedance stage.

This stage has a very simple operation system, on the first clock semi cycle the switch is closed and electrochemical cell current, I_{CELL}, charges capacitor C_S to a concrete output voltage V_{OUT} as depicted in equation 18, where T_{CLK} is the clock period.

$$V_{OUT} = \frac{I_{CELL} \; T_{CLK}}{2C_S} \tag{18}$$

On the second clock semi cycle the switch is opened, and V_{OUT} is directly connected to ground and the capacitor is discharged. Depending on the measurement range, the capacitor or the clock cycle can be modified to a larger or smaller value, giving the possibility of a more versatile stage.

The system operation it is simple, but, as stated in the previous section, we get functionality limitations due to transimpedance amplifier limitations. First of all the WE electrode is ground referenced through amplifier virtual ground. In that case, input offset voltage and input referred noise must be considered in order to provide a steady virtual ground. Since generated current must flow through transimpedance stage, TIA amplifier input bias current should be small and input impedance should be very large in order to minimize any current losses through the stage.

Another important consideration is that the capacitance of the flowing current source, that is the electrochemical cell, must be of a few orders of magnitude higher than the capacitor C_S. If not, the errors due to charge injection will be larger than desirable for any designed application.

This kind of topology is widely used in CMOS processes and microelectronics development due to the difficulty of realizing large resistors at small scales. The fact of using small capaci-

tance values provides the possibility of developing multichannel sensor arrays [11,38,41] on ASIC structures, due to the high degree of integration of small size capacitors.

A more complex development of the switching capacitors technique makes it possible to perform direct A/D conversion by converting the current to variables such as frequency [9,42] or direct current input sigma-delta converter [11,43,44].

3.2. Electrochemical impedance spectroscopy

In section 2.2 the electrochemical cell and its theoretical electrical approximation by circuit modeling was introduced. But this model or other more complex one [45] are just approximations to the reality. A direct measurement of the impedance in a range of frequencies, usually from 1mHz to 1MHz [46], is fitted afterwards to an electrical model, with different elements, that are used to fit the data. In this section the electronics are presented along with the different approaches to extract such measurement, which is defined as Electrochemical Impedance Spectroscopy (EIS).

Current research in biosensor technology has been developed toward better transducers that demonstrate superior sensitivity, portability, accuracy and throughput; where the most promising solution to check the sensor's measurements is based on the use of the EIS technique - the response of an electrochemical cell to small amplitude sinusoidal voltage signal as a function of frequency.

EIS is a more effective method to probe the interfacial properties of the modified electrode, through measuring the change of electron transfer resistance at the electrode surface, caused by the adsorption and desorption of bio-chemical molecules and the antibody-antigen (Ab-Ag) interactions. The measured signal, in this case the signal generated (voltage or current signal) in the experiment, differs in time (phase shift) with respect to the perturbing (voltage or current) wave, and the ratio $V_{CELL}(t)/I_{CELL}(t)$ is defined as the impedance (Z_{CELL}), and accounts for the combined opposition of all the components within the electrochemical cell to the flow of electrons. In this section we will talk about the lock-in amplifier necessary to detect the impedance value of an experience based on an EIS technique.

Measurement of biochemical concentrations is essential for disease diagnose and biological systems characterization. The key electronic component for these measurements, as it is stated before, is the potentiostat amplifier to bias the sensor and read the current produced by the experiment. It is the interface between the biological elements and the lock-in amplifier, which generates the real and imaginary components for the EIS solution rejecting undesirable harmonics and noise interferences [47,48,49,50] even in the presence of high noise level. The block diagram of the whole system is depicted in Figure 12, where a general schematic view of a lock-in amplifier is shown.

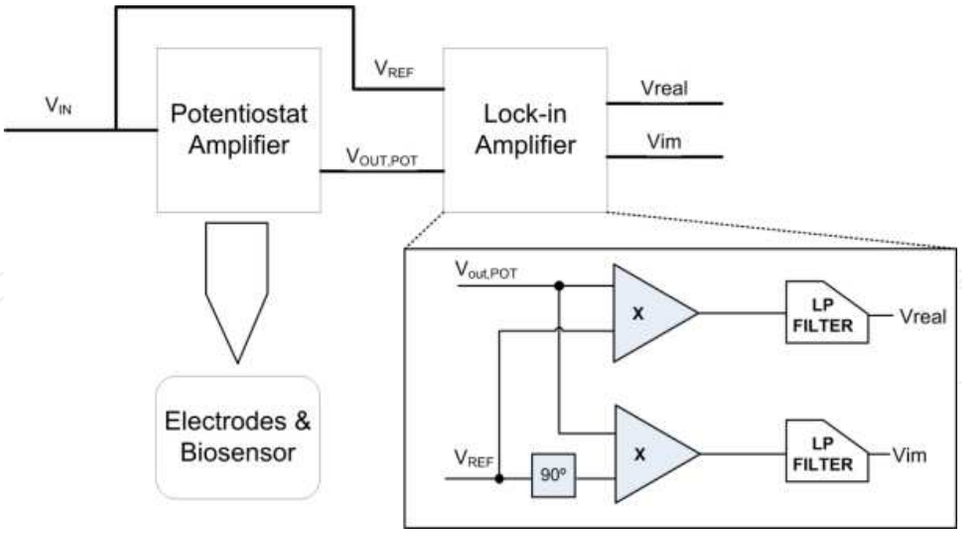

Figure 12. Block diagram view of a complete system of Potentiostat, Biosensor and Lock-in. Schematic view af a Lock-In amplifier.

The basic operation of the Lock-in Amplifier is very simple. $V_{out,POT}$ represents the potentiostat amplifier output signal, so

$$V_{out,POT} = I_{CELL} \cdot R \tag{19}$$

where R is the relation in ohms between the current on the cell and the output potentiostat signal (like R_{TIA} on transimpedance amplifier based potentiostats). Considering the $V_{out,POT}$ function as a frequency dependant, we get:

$$\begin{aligned} V_{out,POT}(t) &= V_{OUT} \sin(2\pi ft + \phi_{OUT}) = \\ &= V_{OUT}[\sin(2\pi ft)\cos(\phi_{OUT}) + \cos(2\pi ft)\sin(\phi_{OUT})] \end{aligned} \tag{20}$$

So, our functions Vreal and Vim are represented by the following equations.

$$\begin{aligned} Vreal &= V_{out,POT} \cdot V_{IN} \sin(2\pi ft) = \\ &= V_{OUT} \cdot V_{IN} \cdot \left(\sin^2(2\pi ft)\cos(\phi_{OUT}) + \tfrac{1}{2}\sin(2\pi ft)\cos(2\pi ft)\sin(\phi_{OUT})\right) \end{aligned} \tag{21}$$

$$\begin{aligned} Vim &= V_{out,POT} \cdot V_{IN} \cos(2\pi ft) = \\ &= V_{OUT} \cdot V_{IN} \cdot \left(\cos^2(2\pi ft)\sin(\phi_{OUT}) + \tfrac{1}{2}\sin(2\pi ft)\cos(2\pi ft)\cos(\phi_{OUT})\right) \end{aligned} \tag{22}$$

$$Vreal = \tfrac{1}{2} V_{OUT} \cdot V_{IN} \cdot [\cos(\phi_{OUT}) - \cos(4\pi ft)\cos(\phi_{OUT}) + \sin(4\pi ft)\sin(\phi_{OUT})] \tag{23}$$

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$$Vim = \frac{1}{2} V_{OUT} \cdot V_{IN} \cdot [\cos(\phi_{OUT}) + \cos(4\pi ft)\sin(\phi_{OUT}) + \sin(4\pi ft)\cos(\phi_{OUT})] \quad (24)$$

Taking into account only the DC component,

$$Vreal = \frac{1}{2} V_{OUT} \cdot V_{IN} \cdot \cos(\phi_{OUT}) \quad (25)$$

$$Vim = \frac{1}{2} V_{OUT} \cdot V_{IN} \cdot \sin(\phi_{OUT}) \quad (26)$$

The magnitude and phase of $V_{out,POT}$ are

$$|V_{out,POT}| = \frac{2}{V_{IN}} \sqrt{V_{real}^2 + V_{im}^2}; \ \Phi_{Vout,POT} = \text{arctg}\left(\frac{V_{im}}{V_{real}}\right) \quad (27)$$

Being the magnitude and phase of impedance Z_{CELL}:

$$|Z_{CELL}| = \frac{V_{IN} \cdot V_{CELL} \cdot R}{2\sqrt{V_{real}^2 + V_{im}^2}}; \Phi_{ZCELL} = \text{arctg}\left(\frac{V_{im}}{V_{real}}\right); \quad (28)$$

3.2.1. The analogue approach

In the previous section have the idea of a whole system based on a potentiostat and a lock-in amplifier as a complete solution for an electrochemical impedance spectroscopy experiment was introduced. In this section, it is presented the configuration of a lock-in amplifier that generates the real and imaginary components of the impedance (Z_{CELL}) based on an analog instrumentation implementation is presented.

The lock-in amplifier architecture based on an analogue approach [48,49,50], consists in different modules, which are two Synchronous Demodulated Channels which generates DC voltage signals which are proportional to the real (V_{real}) and imaginary (V_{im}) components of the input signal (potentiostat measurement). The circuit schematic, with the demodulator and the low pass filter, is depicted in Figure 13, where $V_{out,POT}$ represents the potentiostat amplifier output signal (equation 19).

The lock-in amplifier provides real and imaginary components through the DC values Vreal and Vim, respectively, after filtering the rectified signals from the demodulator stage, getting a complete characterization of potentiostat output signal and an accurate estimation of Z_{CELL} (electrochemical reaction characteristics).

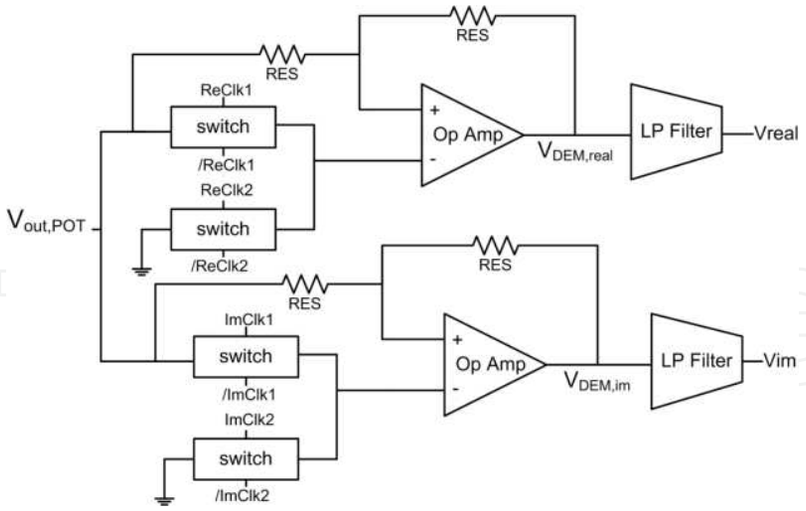

Figure 13. Full schematic view of the implemented lock-in module [58].

Special attention is given to the reference signal used by the demodulator channels which is multiplied by the signal to be measured. The reference (V_{REF}) signal is an ac voltage, of the same frequency of the input signal, which can be either generated by an oscillator, locked to the input signal by a phase locked loop or mainly using the same polarization signal of the previous stages (V_{IN}). A phase shifter allows the reference signal to be trimmed at the following phases: phase ReClk1 = 0º, phase ReClk2 = 180º, phase ImClk1 = 90º, phase ImClk1 = 270º. The clock signals generator is depicted on Figure 14.

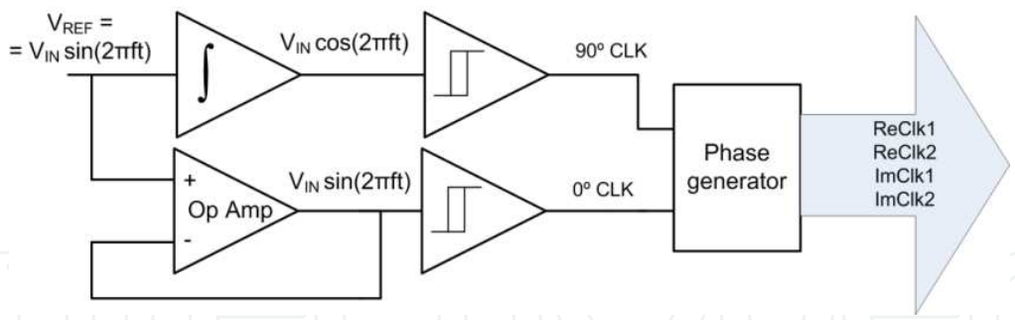

Figure 14. Clock generation module [58].

Clock signals are generated by two hysteretic comparators, one for the 0º phase clock and the other one for 90º phase clock signals, previously generated by an integrator. It's desirable that the different four clock signals be generated with a dead time, DT in Figure 15., between them for each channel, ReClk1 and ReClk2 for V_{REAL} channel and ImClk1 and ImClk2 for V_{IM} channel. The dead time must be implemented in order to avoid undesired spikes at the generated clocks and harmonic distortion coupling on the demodulator channels. Dead time values must be several orders of magnitude less than the clock period to not interfere with the clocks phase shift.

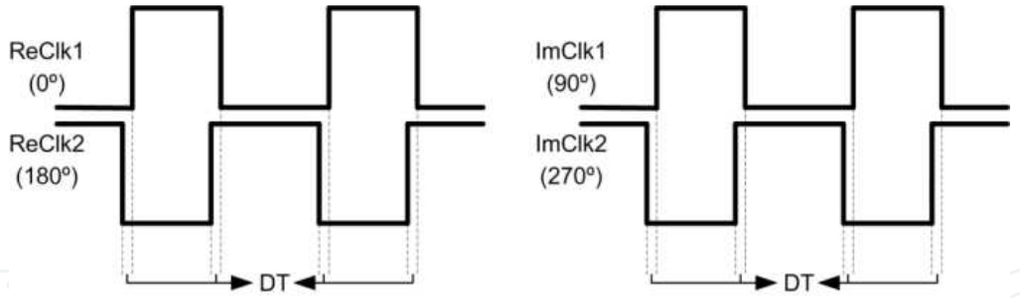

Figure 15. Dead time conceptionClock generation module

Finally, the demodulation stage consists of two simple wave rectifiers. On each rectifier, when the input signal to be measured and the reference signal are of the same frequency, the demodulator output has a dc component proportional to the input signal amplitude [48,49,50]. By adjusting the phase of the reference signal using the phase-shifters present in the reference channel, the phase difference between the input signal and the reference can be brought to zero (null shift procedure). If we get all the four phases; 0º, 90º, 180º and 270º; considering the two different channels on demodulation stage, we have a complete data spectrum to evaluate the whole input signal.

A low pass filter characterized by a low cut-off frequency is necessary to reject the noise and harmonics superimposed to the output demodulation stage and acquire the dc component proportional to the signal. A very interesting architecture is based on a trans-conductance amplifier (OTA), due to the very small trans-conductance values, in the order of nano-siemmens, that can be defined [51]. The basic structure is based on a source degenerated trans-conductance amplifier (OTA) to define the filter. The source degeneration increases the input range of the amplifier and also decreases the equivalent trans-conductance of the OTA amplifier. The ratio between the current mirrors decreases the current level at output, which results in an even minor value [52]. These current mirrors are based on composite transistors, used to reach greater copy factors. The typical transfer equation and cut-off frequency are the following

$$|H_{FILTER}| = \frac{\frac{gm1 \cdot gm2}{C1 \cdot C2}}{s^2 + s \cdot \frac{gm2}{C2} + \frac{gm1 \cdot gm2}{C1 \cdot C2}} \tag{29}$$

$$\omega_0 = \sqrt{\frac{gm1 \cdot gm2}{C1 \cdot C2}} \tag{30}$$

Then, integratable capacitors can be implemented, defining cut-off frequencies in the range of 0.1Hz to 30Hz. The LP Filter on Figure 13. is depicted as a Gm-C second-order low pass-filter in Figure16.

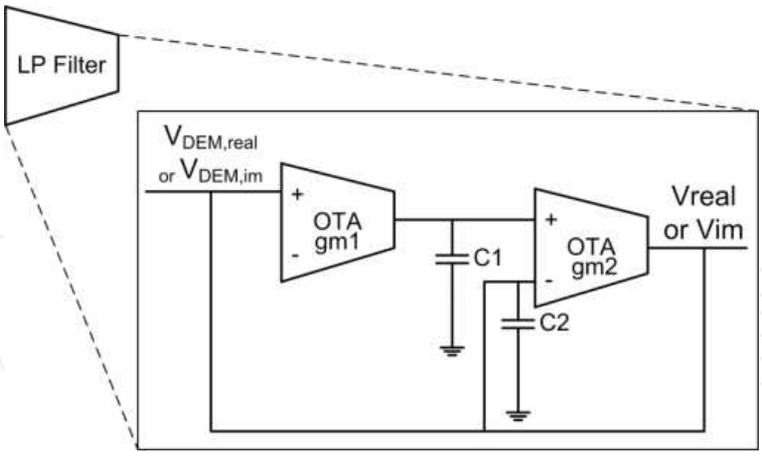

Figure 16. Gm-C Second order filter configuration.

Once we get both real and imaginary components of the measured signal from the analogue lock-in amplifier, we need to process these raw dc values to obtain reliable information about our system to perform an EIS experiment with them. In order to develop a complete system for EIS experiments, the dc raw data on lock-in output must be digitalized in order to carry out the mathematical post-processing, equation 31 to 34, on a microcontroller, DSP or computer. The digitalization of the output data is easiest than in other devices due to the acquisition of only DC signals. The theoretical expression of the module and phase of $V_{out,POT}$, in Figure 13, using the Randles model, are found in following equations:

$$|V_{out,POT}| = \frac{\pi}{2}\sqrt{V_{real}{}^2 + V_{im}{}^2} \tag{31}$$

$$\Phi_{Vout,POT} = arctg\left(\frac{V_{im}}{V_{real}}\right) \tag{32}$$

$$|Z_{CELL}| = \frac{2}{\pi} \cdot V_{CELL} \cdot R \cdot \frac{1}{\sqrt{V_{real}{}^2 + V_{im}{}^2}} \tag{33}$$

$$\Phi_{ZCELL} = arctg\left(\frac{V_{im}}{V_{real}}\right) \tag{34}$$

Where 2/pi is the mean absolute value of the sine function [48].

Obtaining with equation 36 and 37 a direct measurement of both Z_{CELL} module and phase and Z_{CELL} real and imaginary components and obtaining reliable data for Electrochemical Impedance Spectroscopy experience. In Figure 17 the behavior of the demodulation stage for both channels is shown.

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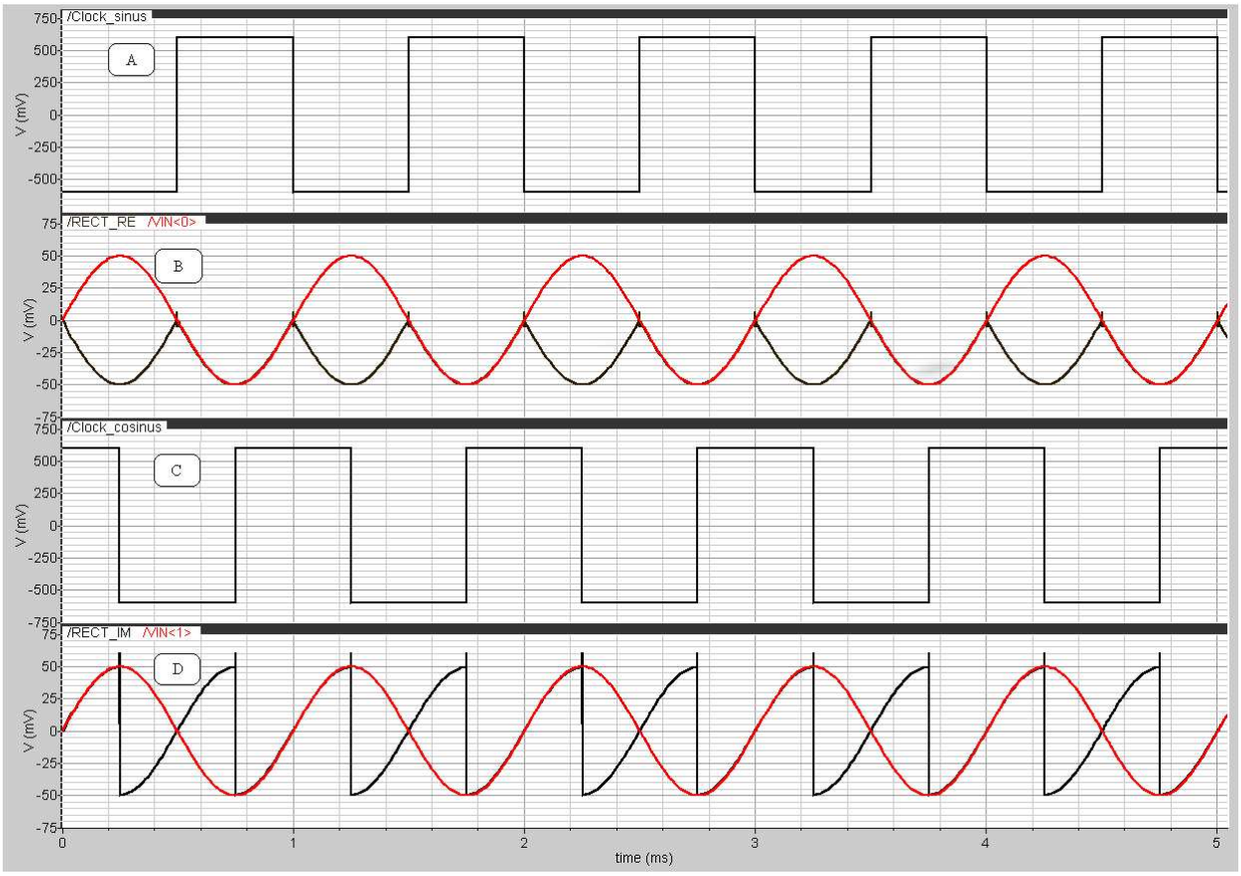

Figure 17. Caption of the rectified signals for the real and imaginary channels before the active filters. Upper trace (A) represents the reference clock signal for the synchronous demodulated channel for the real component, before the filter (Vreal); next figure (B) is the rectified signal. The third signal (C) is the reference clock signal for the synchronoys demodulated signal for the imaginary component (Vim), and the last trace (D) at the bottom, is the trace of the rectified signal at the imaginary channel. These traces are obtained for a 180º condition.

3.2.2. The digital approach

As has been stated in section 3.1.2.3, some potentiostat solutions employ an output digital signal in order to facilitate the data processing and transmission. Since the use of analogue instrumentation processing usually leads to a final data digitalization, the possibility of a direct embedded processing is an interesting approach to developing a lock-in amplifier. The digital lock-in approach is based on an embedded mathematical processing on a microprocessor or DSP device [19,53]. The block diagram of the lock-in software is depicted in Figure 18.

In order to proceed with the signal processing there are two main approaches: a) the Fast Fourier Transform (FFT) [18], and b) the Frequency Response Analyzer (FRA) [19]. In the case of the FFT, a pulse, or a step, -the approach to be followed is the ideal Dirac function-, is applied to the sample because it contains a wide frequency content. Then, the response of the sample is digitalized and processed in a digital processor, for instance a DSP, and using the FFT algorithm, the different frequency components are obtained for their analysis. Another possibility is the logarithmic sampling in the DFFT calculus, reducing the data required in the

process [18]. This appears to be simple, but there are several problems in the implementation. First of all, it is very difficult to generate a fast step function and a very fast potentiostat capable of driving this step on the electrodes and extracting the resulting current signal. If the potentiostat rising time is too slow, the resulting frequency components will be distorted. Since the important information is contained in a short period of time after the step is applied, in addition to a very fast potentiostat, very fast ADC with a high precision bit resolution is also required

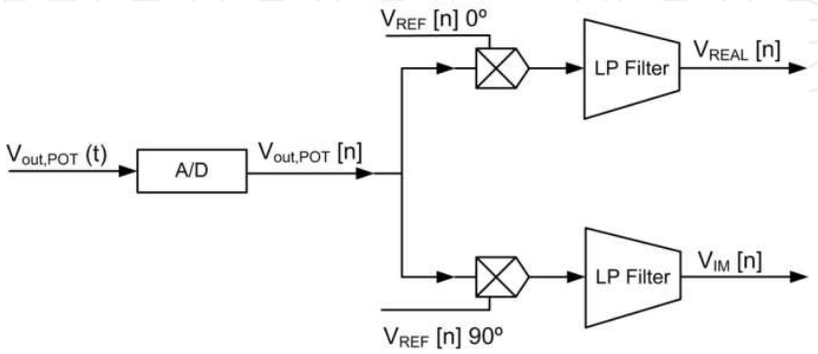

Figure 18. Digital lock-in block diagram.

A simpler solution is based on the FRA approach. In this case a sine and cosine signals are adopted and by means of two multipliers and a filter stage the real and imaginary components of the response are obtained. This measurement must be done for each frequency. Working with just one sensor and in terms of the size of the final product, the FFT option could be adopted, although high speed hardware and heavy algorithm implementation is required, because the response for several frequencies is obtained. The FRA solution is more oriented to multi-sensor approaches but is also a good option in the case of single sensors, in terms of the trade-off between complexity and speed, if not too low frequencies are to be measured.

This lock-in approach is more feasible. The digital lock-in FRA approach [19] is based on the principle that there is no correlation between noise and measured signal. In contrast to the analogue approach, an orthogonal arithmetic multiplying between the incoming potentiostat signal and reference signal are used to get the real and imaginary components, coming close to the theoretical behavior of a lock-in amplifier depicted in section 3.2. A digital lock-in has no low frequency limitations, being capable of working properly at the sub-hertz region. The upper frequency limitation is mainly limited by the ADC conversion time, being able to develop a wide frequency range EIS system. On the other hand, the digital lock-in is limited by area and power consumption. The area and power consumption levels depend on the electronics involved. If a microprocessor is needed, we get typical power consumption, for commercial solutions, of several hundreds of mW, which is far from the desired power waste. But in the recent years a step forward in microprocessors field has been presented in [54] and [55]. [54] Present a microprocessor, in a 180 nm technology, with a power consumption of 226 nW, and area of 915x915 mm^2. It evolved from [55], where the sub-threshold operating region is explored. In the same way there has been an evolution in microprocessor development, in terms of area and power consumption. [19] Present an evolution of the digital lock-in algorithm

based on an oversampling solution, simplifying the orthogonal vector arithmetic cutting off all the multiplying operations.

In that way, evolution of both microprocessor hardware and lock-in algorithm software, leads to a whole post-processing embedded system with great throughput, functionality and versatility without involving a high area or power consumption.

4. An example of a CMOS low power potentiostat amplifier

In this section the design of a CMOS low power potentiostat amplifier using a 0.13μm technology is described. Potentiostat architecture [2,6,56,57], using the described electrochemical model, is depicted in Figure 19.

This structure is based on four amplifiers (Opamp) and two resistors. OP4 is the transimpedance amplifier, which defines the virtual ground voltage of the WE electrode, and provides current-to-voltage conversion such that,

$$V_{out,POT} = - I_{CELL} \cdot R_{TIA} \tag{35}$$

where I_{CELL} is the current through the cell and R_{TIA} the gain defined on the transimpedance amplifier.

OP3 is used to ensure minimal current flow through the RE electrode. It senses the voltage difference between the RE and WE electrodes (virtual ground). This difference is compared by OP2 with the desired V_{IN} voltage, changing the voltage at the AUX electrode and defining a current through the cell in such a way that the voltage difference between the RE and WE electrodes follows the defined V_{IN} DC+AC signal that polarizes the sensitive cell.

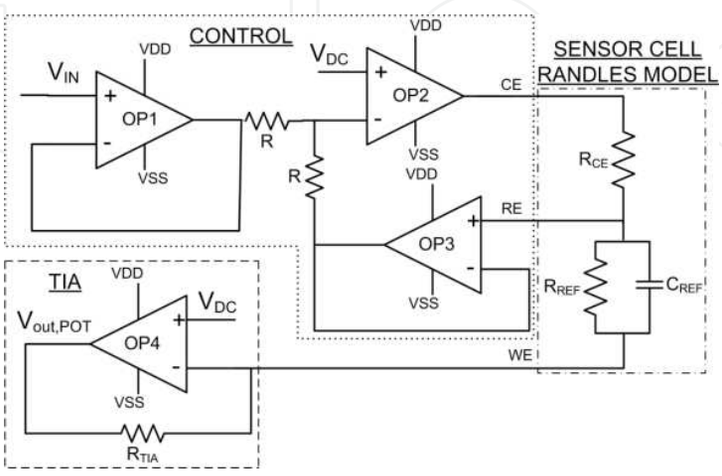

Figure 19. Full schematic view of the potentiostat amplifier with the adopted electrochemical electrical model [58].

If WE electrode is attached at a virtual ground by the transimpedance amplifier, it can be demonstrated that the Zcell impedance, and variations, could be detected continuously by:

$$V_{out,POT} = \frac{R_{TIA}}{Z_{CELL}}(V_{ref} - V_{work}) = \frac{R_{TIA}}{Z_{CELL}} V_{IN} \tag{36}$$

$$Z_{CELL}(j\omega) = \frac{V_{IN}}{V_{out,POT}} R_{TIA} \tag{37}$$

The amplifier adopted to design the potentiostat amplifier is based on a wide-swing, cascode output stage with feedforward class-AB control, Figure 20 and Figure 21, [58-60] for OP1, OP2 and OP3 amplifiers and a full-custom, multi-stage, high input impedance, cascode output stage for transimpedance amplifier OP4. The AB amplifiers (OP1, OP2 and OP3) output transistors have been sized in such a way they can supply the right current for the worst load conditions, defined by the electrochemical model, which has a total value of several MΩ. The input stage of the transimpedance amplifier (OP4) has been designed to increase by three orders of magnitude, the input impedance, minimizing offset and current losses at WE electrode. The power supply is 1.2 V for all the electronics.

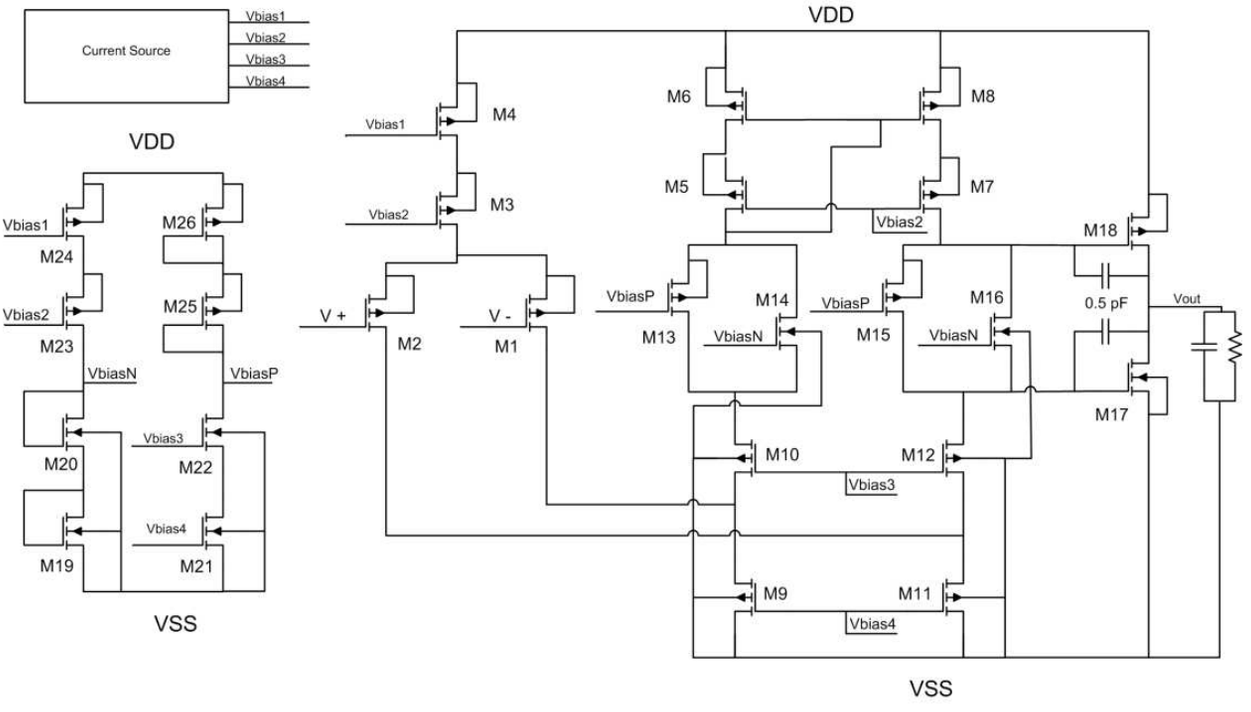

Figure 20. Full schematic view of the AB amplifier [58].

Individual amplifier AB (OP1, OP2 and OP3) is 440μm in height and 500μm in width, with 84 μW of power consumption in nominal conditions (10MΩ@10pF), 108 dB open-loop gain at low frequencies, 300 kHz bandwidth with a PM = 59º and 12 μV of input systematic offset. In Table

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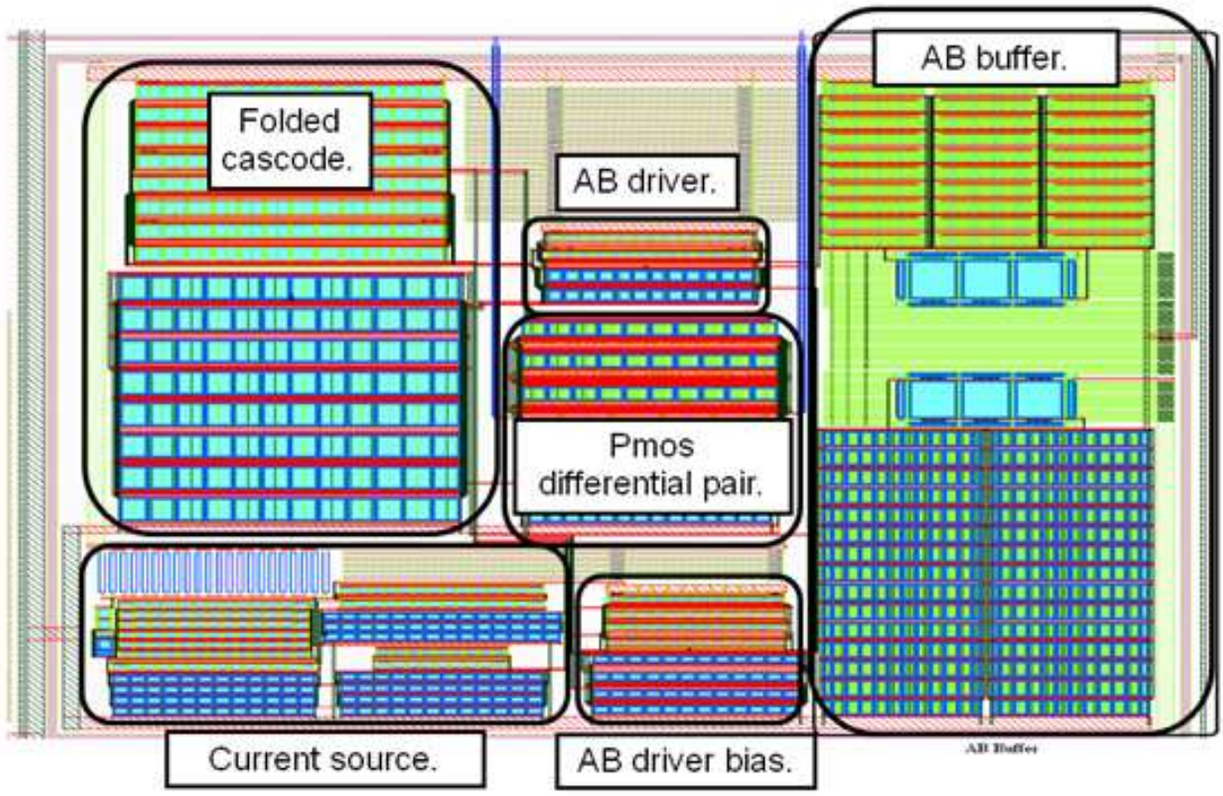

Figure 21. Full layout view of the AB amplifier [58].

1 different results are summarized, based on the typical (TYP), fast (FFA) and slow (SSA) mobility values of the electrical carriers, and for different simulation conditions, are reported.

TYP							
Parameters	V_{offset} (µV)	F_{0dB} (kHz)	Phase Margin (°)	Gain (dB)	V_{noise} (µV)	THD (%)	P_{supply} (µW)
Schematic	-17,56	402,3	60,19	108,9	118,73	5,56m	78,4
Extracted	-12,04	303,7	58,78	107,9	397,15	3,67m	84,9
FFA							
Parameters	V_{offset} (µV)	F_{0dB} (kHz)	Phase Margin (°)	Gain (dB)	V_{noise} (µV)	THD (%)	P_{supply} (µW)
Schematic	-26,07	335,5	65,79	106,1	62,95	1,74m	90,7
Extracted	-17,27	401,7	54,94	108,9	104,44	2,46m	101,9
SSA							
Parameters	V_{offset} (µV)	F_{0dB} (kHz)	Phase Margin (°)	Gain (dB)	V_{noise} (µV)	THD(%)	P_{supply} (µW)
Schematic	-13,83	390,51k	62,12	110,1	62,12	14,49m	95,4
Extracted	-10,42	158,8 k	71,23	102,9	104,49	4,71m	32,1

Table 1. Folded Cascode AB amplifier characterization @ ± 0.6Vsupply

.

Transimpedance amplifier (OP4) is 500μm in height and 1000μm in width, with 61 μW power consumption in nominal conditions(10MΩ@10pF), 85 dB open-loop gain at low frequencies, 400 kHz bandwidth with a PM = 67º and 26 μV input systematic offset.

Taking account of an extremely low offset requirement for bio-implantable devices, this low offset performance is due to an accurate channel length modulation of transistors size at the differential pairs, applying careful techniques for the analogue layout [61]. The linear range of the potentiostat amplifier has been analysed by simulations and it is expected to be 80% of the supply range. As an example; considering a ±100mV full scale voltage, in the ±75mV range the linearity response is quite good, with a deviation error of less than 0.01% [6], as is depicted in Figure 22. The potentiostat amplifier is 1400μm in height and 1000μm in width, with a power consumption of 400μW@$|V_{DD}$-$V_{SS}|$=1.2V.

The full system has been analyzed based on the extracted views of the design. The ranges of the electrochemical parameters are good enough for the targets of the electrochemical cells. Initial simulations of this approach are presented, with positive results in terms of the potentiostat amplifier and lock-in amplifier response. The potentiostat assures a good linearity, and also ensures that the electrochemical cell follows the input voltage V_{IN} as expected. Current losses on the TIA amplifier stage are totally negligible and enclosed.

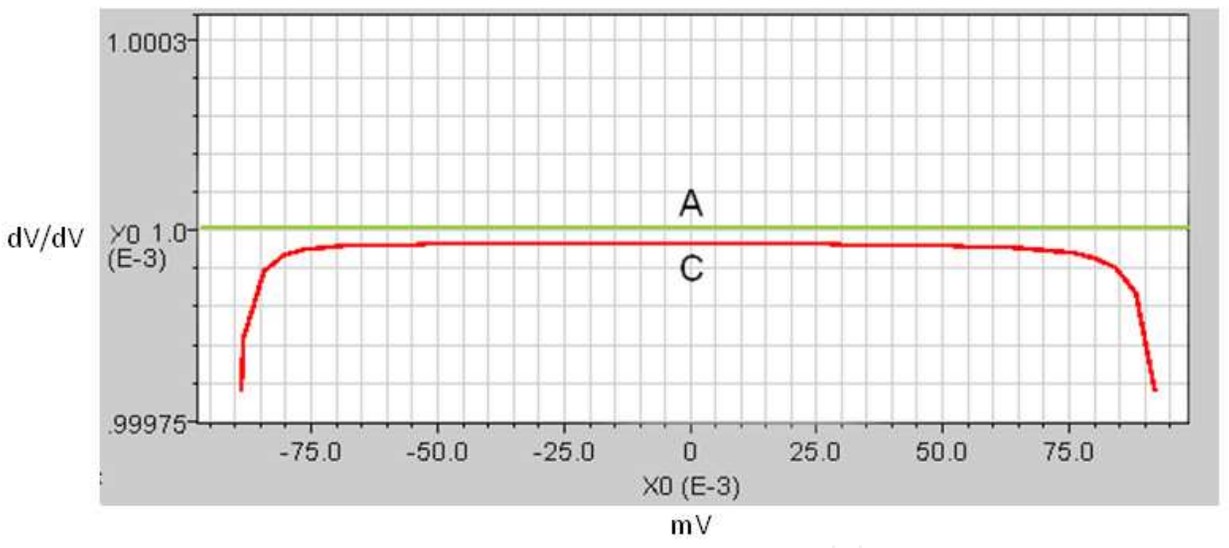

Figure 22. These signals are the derived functions, where A is the input signal (VIN) and C the polarization signal (VCELL).

5. Summary and conclusions

In this chapter, we have introduced the basic principles of biosensors and bioelectronics interfaces specially focused on the design of instrumentation related to amperometrics

biosensors, potentiostat amplifiers and lock-in amplifiers. These elements have been introduced with regard to the state-of-the-art and the trends involved in such systems, and the development of custom built electronic solutions for bio-electronics applications, from discrete devices to ASICS solutions.

Discrete systems are useful for implementation in portable point-of-care applications. As we get less area and power restrictions than an ASIC solution, there are several architectures for data acquisition, processing and transmission. Potentiostat amplifiers can be designed with discrete devices or a monolithic ASIC solution while the lock-in amplifier can be designed with discrete devices or monolithic ASIC for an analogue approach, or an external commercial microcontroller or DSP for a digital approach. We must choose our fit depending on portability, accuracy and reliability requirements.

However, for body sensor networks body or implantable devices development, the increased functionality, reduced systems, with smaller multiplexed electrodes, for ultra-low current detection and versatility will require potentiostat amplifiers to be designed on a system-on-chip (SoC), which will force us to implement the system in CMOS technology.

As stated by [62] a trade-off between versatility and power consumption, aggressive digital processing and analogue data processing or general purpose and custom design, must be considered when developing such systems that integrates medical and electronic technologies. These trade-offs have been presented on this chapter split in two different sections, related to the potentiostat amplifier and to the lock-in amplifier. Finally, an example of CMOS low power potentiostat amplifier has been reported.

Structure Topology	Advantages	Disadvantages
Transimpedance amplifier stage. Section 3.1.2.1.	- Simplicity.	- Virtual ground on working electrode. - Active devices through flowing current path. - Current measurement losses due to amplifier input bias current.
Instrumentation amplifier stage. Section 3.1.2.2.	- No virtual ground on working electrode. No active devices through flowing current path.	- Higher flicker and thermal noise due to extensive use of resistors. - Impedance increase on potentiostat feedback loop. - Low integration degree.
Transimpedance switching capacitor stage. Section 3.1.2.3.	- High integration degree. Most versatile analogue output signal to A/D conversion.	- Virtual ground on working electrode. - Active devices through flowing current path. - Highly dependent on electrode morphology and parasitic capacitors.

Table 2. Summary table section 3.1.

In section 3.1, different potentiostat amplifier topologies have been reported. Different approaches to develop a potentiostat amplifier were introduced, taking account of on every particular situation the pros and contras. Table 2. Choosing the best fit analogue instrumentation has repercussions on several benefits in terms of area and power consumption, and is the first step to a solid efficient design. Exploiting the analogue processing before digitization is the optimal way to develop these systems, regarding all the benefits described.

In section 3.2 the lock-in amplifier is shown with two different approaches, the analogue approach and the digital approach. Table 3.

The analogue lock-in amplifier provides several advantages in terms of post-processing requirement as the digitization of the output data, being a DC signal, is easier than in other kinds of devices, decreasing considerably the complexity of the post-processing and data transmission electronics. On the other hand, this analogue approach has some limitations in terms of versatility and bandwidth, which is limited by the whole lock-in electronics. Assuming the implementation of a CMOS monolithic solution for a whole implantable device, versatility and bandwidth limitations can be acceptable in terms of an efficient custom system.

The digital approach of a lock-in amplifier allows us to develop a very versatile and powerful device. The bandwidth of this system is only limited by the analogue to digital converter and data transmission electronics if needed. The digital lock-in approach being a whole mathematical embedded system can be implemented in different processing topologies, such as real time processing by means of a FPGA (Field Programmable Gate Array), or standard processing by means of a DSP or microprocessor. A digital lock-in has no low frequency limitations, being able to work effectively at the sub-hertz region. The upper frequency limitation is mainly limited by the ADC conversion time, being capable of developing a wide frequency range EIS system.

Structure Topology	Advantages	Disadvantages
Analog lock-in. Section 3.2.1.	- Simplest analog output signal A/D conversion. - Less power and area consumption.	- Low and high frequency limitation. - Pure AC signals needed.
Digital lock-in. Section 3.2.2.	- No frequency limitation. Wide frequency range operation. - More versatile system.	- Higher power and area consumption due to ADC or microcontroller.

Table 3. Summary table section 3.2.

We must keep in mind the large area and power increase represented by a microprocessor, DSP or FPGA, which can make this lock-in approach not suitable for low power consumption electronics or implantable devices. However, as it has been reported in section 3.2.2, advances in DSP area and power requirements and advances in digital lock-in algorithms have made the possibility of a digital lock-in implementation on a low-power system-on-a-chip CMOS implantable device feasible.

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