Synthesis and characterization of In_2O_3 nanostructures

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Abstract: The growth of In_2O_3 nanostructures via Volmer-Weber growing process, using metallic indium as the precursor and Ar or Ar/O_2 gas mixture as the carrier gas, has been carried out. The effect of the growth temperature, pressure, gas flow and the role of the presence of a catalyst (Au) has been studied by structural, electrical, and optical characterization techniques. The results show a correlation between the measured resistance and bandgap with the microstructural characteristics of the grown layers.

I. INTRODUCTION

Metal-oxides are very interesting semiconductor materials whose synthesis and device fabrication have attracted a lot of attention in the last decades due to the possibility to tune their physical properties [1]. Among them, In_2O_3 is a n-type wide bandgap semiconducting material that has been widely used in gas sensors and optoelectronic devices, such as solar cells and liquid-crystal displays, owing to its high optical transparency to visible light and low resistivity. It is well known that In_2O_3 nanostructure's properties strongly depend on their morphology, reason why their preparation with specific morphologies is required to accomplish different scientific and technological needs. For example, nanowires have been widely used as gas sensors due to their large surface-to-volume ratio and to the strong interaction between some gas molecules and In_2O_3 surfaces. Less attention has been paid to the controlled growth of nanostructures with other morphologies [2, 3]. Therefore, the study of the experimental conditions needed to obtain specific types of nanostructures can be interesting for potential practical applications.

The present study is focused on the growth of In_2O_3 nanostructures using metallic indium as the precursor and employing different experimental conditions on bare or Au sputter-covered Si/SiO_2 pieces or fused silica integrated circuits (ICs) samples. The synthesized material has been characterized structurally, electrically, and optically.

II. EXPERIMENTAL

A. In_2O_3 Growth

Prior to any experiment, samples and holders must be cleaned with isopropanol to avoid a large part of potential contamination. Next, 0.15 ± 0.01 g of metallic In (precursor) is placed in a fused silica boat, which is placed next to an inverted alumina boat, on top of which the samples are uniformly placed, as can be seen in Fig.(1). The substrates on which the growth will be studied are placed always at the same point on the alumina inverted boat to perfectly repeat the experiment, if needed. Both fused silica and alumina boats are introduced in a 5 cm diameter quartz tube inside the furnace. To carry out the evaporation of the precursor and the deposition on the substrates, high temperature is applied to the furnace.

The growth process is carried out under different conditions of pressure, temperature and gas flow in order to study the optimal conditions for the different In_2O_3 nanostructures which can grow. The dimensions of the 2 nm-thick sputter-covered Au on 620 nm Si/SiO_2 samples were 5x5 mm^2.

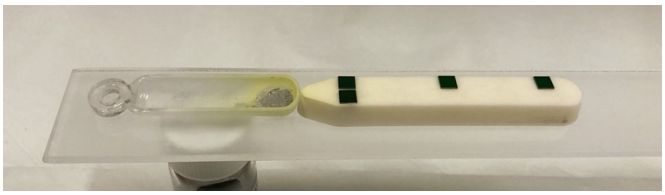

FIG. 1: Image of the precursor (left) and Si/SiO_2 substrates (right), as introduced into the furnace.

Once the samples are introduced into the tube, this is pumped down in order to eliminate non desirable gases, especially water vapor, reaching a vacuum level of 2 mtorr. Then, the furnace is heated for 1 h at a constant heat rate to reach the selected temperature, which is maintained for 60 minutes, followed by the natural cooling of the system. A constant gas flow is provided during the whole process, being either pure Ar or a mixture of Ar and a reduced concentration of O_2 of 0.1%, at most. Pressures below 760 Torr are maintained throughout the experiments by a vacuum pump, which is connected to an automatic pressure control system.

The growth of In_2O_3 was performed on bare and on Au sputter-covered Si/SiO_2 substrates or integrated circuits (ICs) made of deposited Ti/Au (10/50 nm) on top of fused silica substrates. The latter are shown in Fig.(2). The dimensions of these chips are 6x10 mm^2 and contain 2 pads and interdigitated electrodes, of 10 μm width and separated 10 μm. The growth process is the same, except for the cleaning, which used first acetone, followed by isopropanol, to eliminate possible rests of adhesive, and finished drying with N_2 gas. Before the introduction in the furnace, all the ICs have also been

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electrically measured to verify that no short circuit exists between the two pads.

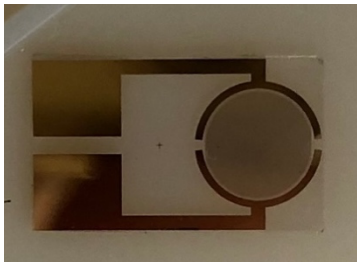

FIG. 2: Image of a fused silica IC, where the pads (left) and interdigitated electrodes (right) can be seen.

B. Characterization

All the fabricated samples have been analyzed in a Jeol 7100F or a Jeol 7001F Field Emission Scanning Electron Microscopes (SEM), operating at 5 kV. This is one of the most commonly used techniques to characterize materials and allows to study the structural characteristics of the deposited semiconducting oxide as a function of the growing conditions.

An UV-VIS spectrophotometer (Specord 205, Analytik Jena) has been used to determine the optical properties of the In_2O_3 nanostructures grown on the fused silica ICs.

The resistance of nanostructures grown on the ICs has been investigated by applying an electrical current to the pads and measuring the voltage drop using a source measurement unit (SMU) (Keithley 2602B).

III. RESULTS AND DISCUSSION

A. Structural characterization

Different nanostructures have been grown on bare and Au sputter-covered Si/SiO_2 samples by varying the experimental conditions. In particular, temperatures in the range of 750-900 °C, pressures between 10 and 760 Torr (atmospheric pressure) and O_2 concentrations up to 0.05 % have been used to synthesize three types of nanostructures that we could name: *nanoworms*, *nanostones* and *nanoswords*, which are shown in the SEM images of Fig.(3). The experimental conditions for synthesizing the different nanostructures are summarized in Table I. It is important to mention that at low temperatures and pressures the simultaneous formation of *nanoworms* and *nanostones* occur.

TABLE I: Experimental conditions of temperature (T), pressure (p), flow of Ar and concentration of O_2 for growing the different types of nanostructures.

	Nanoworms	*Nanostones*	*Nanoswords*
T (°C)	800-900	800-900	750-850
p (Torr)	10-760	10-760	100
Flux Ar (sccm)	100	100-500	500
% O_2	0	0.0-0.02	0.004-0.05

Regarding the synthesis of *nanostones*, they present different sizes, shapes, densities, uniformity in their dimensions and the formation of a layer or the isolated growth of isolated nanostructures have been observed. In particular, Fig.(3)b shows different shapes and sizes of isolated *nanostones*, while in Fig.(3)c a homogeneous layer of smaller nanostructures can be observed.

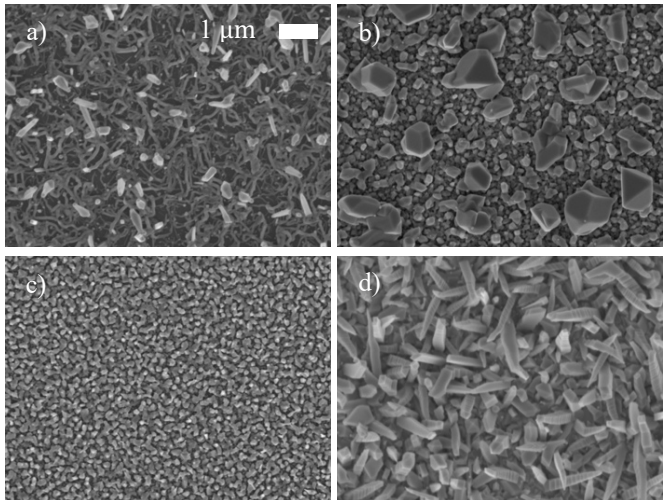

FIG. 3: SEM images corresponding to the In_2O_3 growth of a) *nanoworms*, b) different shapes and sizes of isolated *nanostones,* c) a homogeneous layer of *nanostones*, and d) *nanoswords*. The size bar is the same for all images.

Prior to growing In_2O_3 on the ICs, a thermal treatment has been carried out on them to verify their stability during the high temperature process. In general, the wide metallic lines, like the pads, are quite stable and do not show important structural changes, while the narrower lines, like the interdigitates, are strongly affected. Fig.(4)a shows the SEM image of an unheated IC, where the electrodes appear dark. Fig.(4)b shows that Au island formation occurs when heating the fused silica IC to 900 °C. The heating causes the thermal activation of Au atoms, which flow around at the substrate surface and nucleate into droplets [4].

After this test, the same experimental growth conditions were used on different ICs, either with 20 s sputter-covered Au or without Au, to compare the nanostructure formation as a function. In particular, the conditions of flow of 500 sccm, O_2 concentration of 0.05 %, temperature of 900 °C and pressure of 100 Torr were used. Even though all the grown

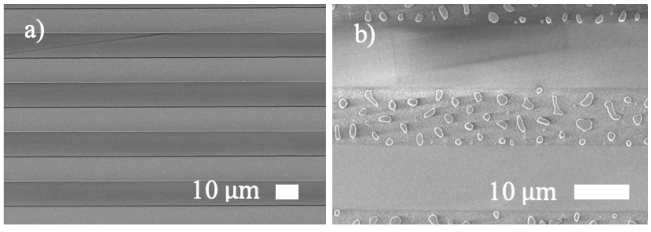

FIG. 4: SEM images of the fused silica ICs a) untreated, and b) heated to 900 °C, evidencing the formation of Au droplets.

material is identified as *nanostones*, their shape and size vary in the different areas of the chip shown in Fig.(2). In particular, the nanostructures synthesized on top of the electrodes show different sizes and densities than in the rest of the chip. As the latter is more comparable to the behavior on the Si/SiO_2 substrates, in the present study the attention will be focused on the non-electrode parts and the electrical and optical characterization will be performed in these areas.

Fig.(5)a shows that two sizes of nanostructures have been grown on bare fused silica ICs, while more uniform and smaller nanostructures have been synthesized on Au sputtered-covered IC, shown in Fig.(5)b. The SEM cross-section images of the two samples, obtained using Focused Ion Beam (FIB) system, Fig.(5)c and Fig.(5)d, respectively, allow to visualize the different homogeneity and density of the grown nanostructures in both layers. While a low density of larger nanostructures has been synthesized on bare ICs, which evidence the presence of holes, it can be observed in Au sputtered-covered samples a high density of smaller nanostructures forming a uniform layer, shown in Fig.(5)d. Therefore, it can be concluded that the presence of Au stimulates the formation of a denser layer of a unique shape of smaller *nanostones*. A possible explanation could be that a concentration of Au nanoparticles (NPs) could promote the efficiency of agglomerating and coalescing, fact that would cause the increase of the layers' density [5].

The synthesis of the nanostructures is supposed to be by Volmer-Weber growth. This method consists in the growth of isolated deposits due to the greater bonding energy with other nanostructures compared to their adsorbed energy to the substrate. As a result, small nuclei are created, which impinge upon one another to finally coalesce, creating a continuous film [6]. This process is briefly summarized in Fig.(6).

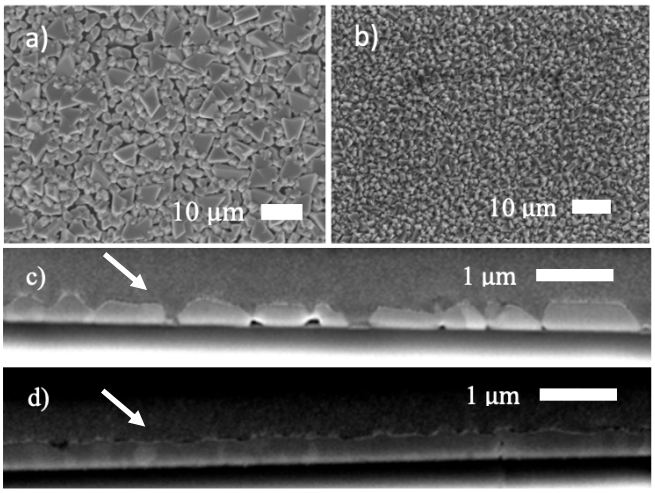

FIG. 5: Top-view SEM images of the In_2O_3 synthesis on a fused silica part of a) bare, and b) Au sputter-deposited fused silica IC. Cross-sectional SEM images, prepared inside a FIB, of the c) bare, and d) Au sputter-deposited fused silica IC cut, showing the In_2O_3 layer morphology. The arrows in c) and d) point out the In_2O_3 layer.

FIG. 6: Sketch of the Volmer-Weber growing process [6].

B. Electrical characterization

The V-I dependence of the ICs have been measured applying an electrical current between -100 nA and 100 nA to their pads and recording the resulting electrical voltage drop.

First, it has been observed that the V-I dependence follows the Ohm's law at room temperature, so that we can assume that the voltage drop occurs at the semiconducting material. The resistance of the samples has been calculated from the slope of the V-I curve, obtaining the following results: $R_{Non-Au} = 18\ k\Omega$; $R_{Au} = 1\ k\Omega$. Therefore, we can deduce that the presence of Au on the samples gives rise to an important increase of its conductivity. This could be caused by the incorporation of Au into the materials and/or by the different homogeneity and density of the nanostructures between both samples, which can be observed in the cross-section SEM image of Fig.(5)c and Fig.(5)d. From a structural point of view, the presence of holes, the different observed dimensions and the larger nanostructures observed in samples grown on bare fused silica ICs can account for the lower conductivity, while smaller nanostructures and a denser layer allows a better conduction of the current [7].

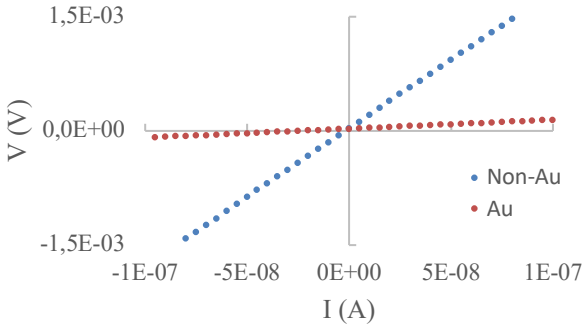

FIG. 7: V-I curves of the grown In_2O_3 on bare (blue) and on Au sputter-covered fused silica IC (red).

Since the V-I curves follow an ohmic behavior, the resistivity can be calculated from considering the geometrical parameters, the measured resistances of the samples and the following equation:

$$\rho = R \cdot \frac{A}{L} \qquad (1)$$

where R is the resistance, A is the cross-sectional area and L is the distance between the electrodes. For this calculation, it is necessary to know the average layer thickness of both

samples. The cross-sectional SEM images of Fig.(5)c and Fig.(5)d, allow to calculate the average layer thickness of In_2O_3 synthesized on bare and Au sputtered-covered fused silica ICs to be approximately 200 nm.

In this way, the resistivity calculated for both samples is $\rho_{non-Au} = 0{,}63\ \Omega \cdot cm$ and $\rho_{Au} = 0{,}03\ \Omega \cdot cm$. Even though these values are slightly larger than the resistivities reported in literature, it is important to point out that they are of the same order of magnitude [8]. Since In_2O_3 is a n-type semiconductor, the concentration of free carrier electrons, n, can be computed with the following expression:

$$n = \frac{1}{q\mu_n\rho} \qquad (2)$$

where q is the elementary charge and μ_n is the mobility of the electrons. Due to the lack of data from these samples, for the calculation we use a reported value of $\mu_n \approx 10\frac{cm^2}{Vs}$. The following results have been obtained: $n_{non-Au} = 10^{18}cm^{-3}$ and $n_{Au} = 10^{19}cm^{-3}$, which are higher than reported in literature [9]. A more accurate result would require the independent determination of the experimental mobility, which is beyond the scope of this work.

C. Optical characterization

The bandgap of the grown In_2O_3 on Au sputter-covered and Au-free fused silica ICs have been determined through UV-VIS spectrophotometry.

First and foremost, the transmittance of the sample holder was measured to know the spectral emission of the lamp, which was repeated at the end of the experiment, after measuring all samples. Three transmittance measurements were made: fused silica IC (T_{IC}), In_2O_3 grown on fused silica IC ($T_{IC+nanostr}$), and In_2O_3 grown on Au sputter-deposited fused silica IC ($T_{IC+Au+nanostr}$).

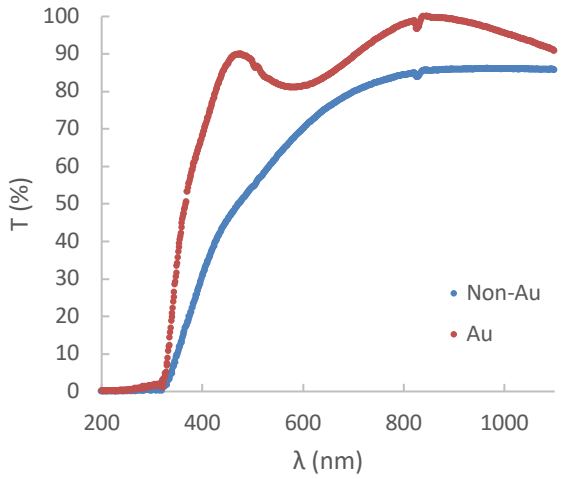

FIG. 8: Normalized optical transmittance of In_2O_3 on bare (blue) and on Au sputter-covered fused silica IC (red).

Fig.(8) shows the calculated transmission spectra after subtracting the substrate contribution. First, it can be observed that the transmission starts at about 320 nm, from which we can have a first estimate of the bandgap value (~3,75 eV). Then, an absorption peak (dip in the transmission) can be seen at about 585 nm in the grown In_2O_3 on Au sputter-deposited fused silica IC but not on the bare sample. This may be caused by a surface plasmon absorption. Surface plasmons are collective excitations caused by the interaction of light with free electrons in metallic nanostructures. It is reported that Au NPs with a diameter of 99 nm exhibit absorption peaks due to plasmon resonance at 575 nm, which is close to the measured value [10]. The differences could be caused by the different amount, size and shape of the Au NPs in our sample. The dips observed at around 830 nm in both samples are due to a change in the detector.

The absorbance, αd (α is the absorption coefficient), is computed with the help of the following expression:

$$\alpha d = \ln\left(\frac{T_{IC}}{T_{IC+nanostr}}\right) \qquad (3)$$

The bandgap, E_g, of a synthesized nanostructure can be determined by representing the Tauc Plot, which is given by following equation [11]:

$$(\alpha d h\nu)^{1/\gamma} = B\left(h\nu - E_g\right) \qquad (4)$$

where h is the Planck's constant, ν is the frequency of the incident photons, B is a constant and γ is an index which can be 2, 3, ½ or 1/3 corresponding to indirect allowed, indirect forbidden, direct allowed and direct forbidden transitions, respectively.

In our case, the best fitting was obtained by plotting $(\alpha h\nu)^2$ vs $h\nu$, as shown in Fig.(9), from which we deduce that In_2O_3 nanostructures present a direct allowed transition ($\gamma = 1/2$) and the value of the bandgap is determined as the

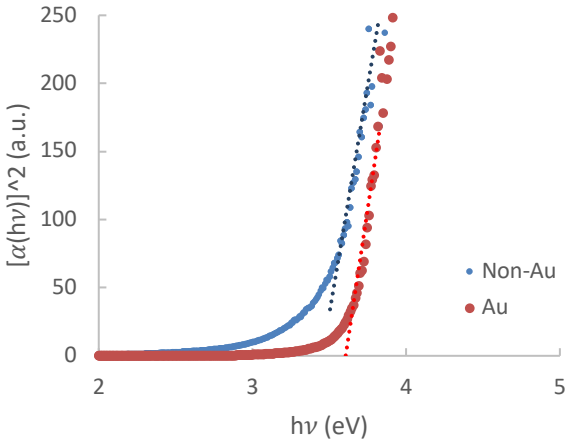

FIG. 9: $(\alpha h\nu)^2$ vs $h\nu$ (Tauc plot) used to determine the optical energy bandgap of the nanostructures grown on bare (blue) and on Au sputter-covered fused silica IC (red).

crossing point between the fitting of the linear part of the plot and the x-axis. The bandgap of In_2O_3 grown on bare fused silica IC was found to be (3.45 ± 0.10) eV, while on Au sputter-covered fused silica IC was (3.61 ± 0.10) eV, which is in good agreement with the values reported in literature [3, 8]. From this we can conclude that the optical bandgap increases when Au has been sputtered prior to the growth. Possible reasons are the smaller size of the nanostructures synthesized on Au sputtered-covered samples, as shown by SEM in Fig.(5)b and in agreement with literature data [10].

IV. CONCLUSIONS

In this work, three different morphologies of In_2O_3 nanostructures have been successfully synthesized on bare or on Au sputter-covered Si/SiO_2 or fused silica ICs by Volmer-Weber technique using metallic indium as a precursor and different experimental conditions. The structural characterization shows that the presence of Au stimulates the formation of a single type of smaller nanostructure, namely *nanostones*.

The grown *nanostones* on fused silica have been electrically and optically characterized. From the electrical characterization we can conclude that the Au sputtering causes a decrease of the nanostructure's resistance, probably the result of the gold incorporation into the layer and the denser and more homogeneous synthesized nanostructures. An estimation of the resistivity and concentration of free electron carriers in the synthesized nanostructures have also been obtained: $\rho_{non-Au} = 0{,}63\ \Omega \cdot cm$ and $n_{non-Au} = 10^{18} cm^{-3}$ for bare substrates and $\rho_{Au} = 0{,}03\ \Omega \cdot cm$ and $n_{Au} = 10^{19} cm^{-3}$ for Au sputtered-covered ICs. The optical results show an increase of the bandgap with the presence of gold and confirm the In_2O_3 direct bandgap of about 3.45-3.6 eV, in agreement with data from literature.

Finally, I would like to include that this work has allowed me to learn new techniques and improve the knowledge acquired during the bachelor's degree.

Acknowledgments

I would like to sincerely acknowledge Dr. Albert Romano for teaching me the different characterization techniques and guiding me on how to do this project. His unceasing help, patience and enlightening advises have let me enhance my background in applied physics.

This project could have not been accomplished without the assistance of Dr. Paolo Pellegrino, who taught how to synthesize In_2O_3 nanostructures and helped me with UV-VIS spectrophotometry.

Last but not least, I would like to be grateful with my family and friends to encourage me every day and give me support during these months.

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