Electronics design for a high precision image stabilization system

A. Casas[a], D. Roma[a], M. Carmona[a], J.M. Gómez[a,c], J. Bosch[a], M. López[a], J. Sabater[a,c], A. Herms[a], T. Maue[b], E. Nakai[b], R. Volkmer[b], W. Schmidt[b]

[a] Universitat de Barcelona, Electronics Department, Martí i Franquès 1, 08028 Barcelona, Spain

[b] Kiepenheuer-Institut für Sonnenphysik (KIS), Schöneckstraße 6, 79104 Freiburg im Breisgau, Germany

[c] Institut de Ciències del Cosmos, Universitat de Barcelona (IEEC-UB), Martí Franquès 1, 08028 Barcelona, Spain

ABSTRACT

A very high precision Image Stabilization System has been designed for the Solar Orbiter mission. The different components that have been designed are the Correlation Tracking Camera (CTC), Tip-Tilt controller (TTC) and the system control in order to achieve the specified requirements.

For the CTC, in order to achieve the required resolution of 12 bits and reduced power consumption, we used an external ADC.

For the TTC, a special focus has been dedicated to a 55 V linear regulator in a QUASI-LDO configuration and a Tip-Tilt driver in a transconductance amplifier architecture.

Results show that the full system reaches an attenuation of 1/10th of a pixel at 10Hz. The TTC provides a high voltage span, enough slew-rate and the needed stability levels.

Keywords: Electronics design, Solar Orbiter, Polarimetric and Helioseismic Imager, Image Stabilization System, Tip-Tilt controller, Correlation Tracking.

1. INTRODUCTION

The Polarimetric and Helioseismic Imager (PHI) Instrument of the Solar Orbiter (SO) mission[1] requires a highly stable sequence of images. Therefore an Image Stabilization System (ISS) with a very high precision has been designed and developed. The system is based on a Correlation Tracking algorithm (CT). The Correlation Tracking Camera provides images that are processed using this algorithm, and detects displacements with subpixel resolution. Based on these measurements, the system will act over a high resolution telescope to change its orientation.

A similar system has already been built and described for the other missions, like B-SOLAR[2], SOHO[¡Error! No se encuentra el origen de la referencia.] and STEREO[4] missions.

In the next sections, we will describe how the ISS has been designed to perform its function with the imposed requirements.

2. SYSTEM DESCRIPTION AND REQUIREMENTS

The PHI instrument for SO mission is one of the remote-sensing units of the SO unit. One of its objectives is to generate high-resolution spectropolarigrams of the Sun. A functional block diagram of PHI can be seen in Figure 1.

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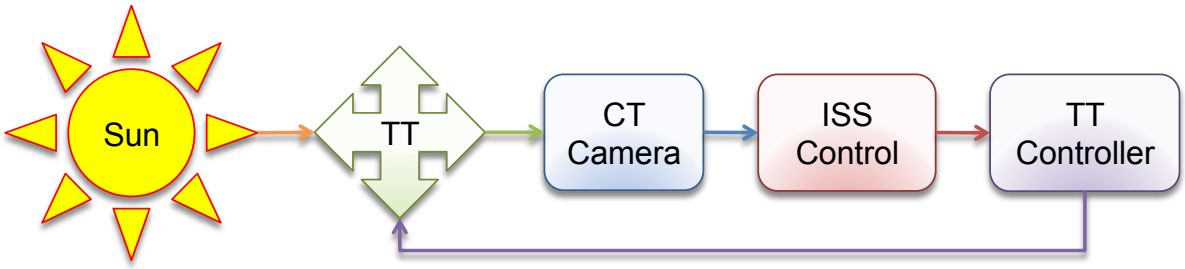

Figure 1. Functional block diagram of the PHI instrument.

The system is based on two telescopes: a High Resolution Telescope (HRT) and a Full Disk Telescope (FDT). Both telescopes share the same APS (Active Pixel Sensor) camera.

To generate a spectropolarigram the system has to take images at different polarization modulations and wavelengths. The minimum number of observables is 4 polarization images at six different wavelengths. To improve the quality of the images, more than one image is taken for every state. These images with the same state are accumulated to increase the Signal to Noise Ratio (SNR). The APS is expected to take an image every 125ms. Every group of different polarizations is taken in 0.5sec. A whole group of images is taken in a cadence of 45-60 sec. As the system calculates differences between images, a good alignment between them is required in order to minimize noise.

The misalignment error has to be below 1/25th of a pixel within the capture of a set of images that provide the spectropolarigram. For this reason, the required HRT pointing stability is 0.02 arcsec within 10s. The FDT needs a stability of 0.2 arcsec within 10s. To measure the HRT 0.02 arcsec, it is necessary, at least, a resolution of 0.01 arcsec. To correct all these instabilities, the instrument includes an Image Stability System (ISS) that is in charge of achieving the 0.02 arcsec stability. This system is based on two tip-tilt mirrors that are properly moved to correct the instabilities.

For corrections of the spacecraft (S/C) movements during the image capture process, a camera is used for detection of the relative displacement of the S/C in relationship with the Sun's surface. The chosen ISS solution is based on a correlator tracker (CT) that controls tip-tilt mirrors to correct the drifts. In this work, the electronics developed for this purpose will be presented.

3. CORRELATION TRACKING CAMERA

The Correlation Tracking Camera (CTC) system is based on the processing of the images taken from STAR1000 image sensor[5]. The block diagram of the CTC is shown in Figure 2.

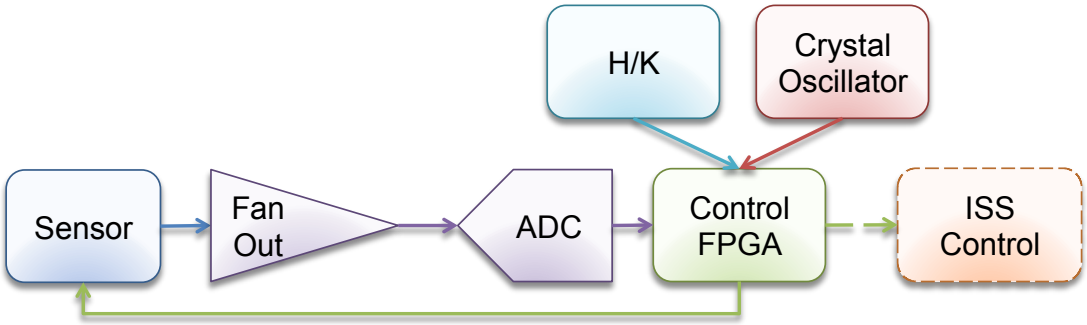

Figure 2. Block diagram of the CTC.

An analog chain is needed to adapt the signal obtained from the image sensor to the ADC input for the FPGA.

3.1 Image sensor

It consists of a STAR1000 image sensor from ON Semiconductor[5]. This sensor has 1024x1024 pixels, with a pixel size of 15 μm x 15 μm. Nevertheless, the size of the images taken is 128x128 pixels. In this way, a rate of more than four-hundred images per second can be obtained.
Although this sensor has a built-in ADC, it only has 10 bits of resolution, making it useless for our purpose, as we need a minimum of 12 bits. Also, it has a high power consumption.
The analog output of the sensor will always have a range from 1.5V to 3.67V, where we have taken into account aging and temperature factors. Therefore, our ADC will have to cope with this range of voltages. Moreover, this analog output has a 100 Ω impedance and is current-limited during transition of pixels. Hence, we have adapted this output by adding a follower amplifier at a first stage, and a fully-differential amplifier in balanced mode at a second stage for obtaining a differential signal. This last stage is shown in Figure 3.

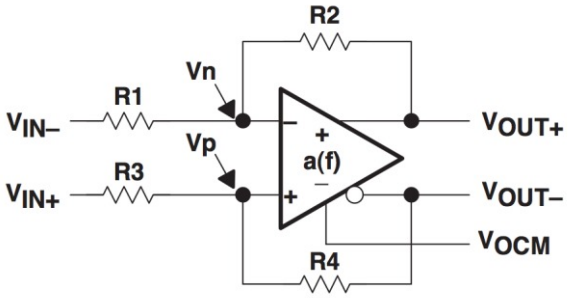

Figure 3. Fully differential amplifier.

In this way, we improve the Signal-to-Noise Ratio (SNR) of the sensor output. We have chosen the resistances in order to have the maximum possible output voltage range. For this we have used the expression for the output voltage of this amplifier:

$$V_{OD} = V_{OUT+} - V_{OUT-} = (V_{IN+} - V_{IN+}) \cdot \frac{1-\beta}{\beta} \quad (1)$$

where,

$$\beta = \frac{R_1}{R_1 + R_2} = \frac{R_3}{R_3 + R_4} \quad (2)$$

R1 is recommended by the manufacturer to be 499 Ω in this configuration. Therefore, we can obtain R2, providing a value of 422 Ω. In this case, as the input voltage range is 2.17V, the output voltage range will be 1.835V.

3.2 Image ADC

We have chosen for the ADC conversion of the image the RHF1201 component[6], from ST Microelectronics. This is a 12 bit low power consumption ADC that allows up to 50 Msps, although a maximum rate of 7 Msps will be used. We have also to take into account that the ADC conversion has a 5.5 clock cycles delay between the analog input and the digital output.

3.3 FPGA

The FPGA device selected for managing the CT Camera functionalities is the Microsemi (Actel) RTSX72SU[7]. It's an antifuse FPGA with a 0.25 um CMOS technology, allowing low power consumption. All its registers are D-type flip-flops with asynchronous SEU (Single Event Upset) robustness (Figure 2-2) and SEL (Single Event Latchup) immunity. The used power supply is 2.5V for the core and 3.3V for the I/O. The FPGA communicates with the ISS through LVDS. In this case, the voltage levels have to be adapted. This adaptation is performed by 400 Mbps transceivers.

4. TIP-TILT CONTROLLER

The Tip-Tilt Controller (TTC) acts over two piezo-drivers for attitude correction. Therefore, high voltages at relatively low frequencies are needed. Moreover, a low current supply for the piezo-drivers must be guaranteed. For solving this problem, an amplifier based on an operational amplifier has been chosen, with an output buffer based on MOSFETs, but controlled by bipolar transistors. A diagram of the TTC is shown in Figure 4.

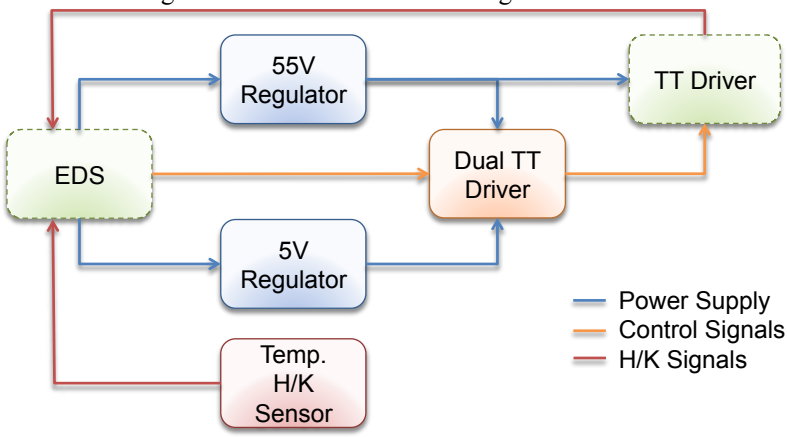

Figure 4. Block diagram of the TTC.

We will be focused on two key elements: the 55V voltage regulator and the dual TT Driver.

4.1 55V voltage regulator

For supplying the circuits with a highly stable voltage, a 55V linear regulator has been implemented in a QUASI-LDO configuration, as shown in Figure 5.

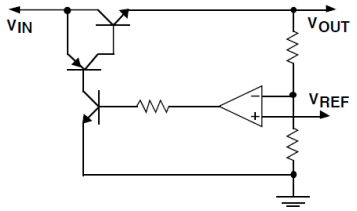

Figure 5. Schematics of a QUASI-LDO configuration

This configuration has been chosen based on the requirements of the regulator. To this regulator, we have added an input filter that eliminates the input noise and ripple of the 60V DC input line and an output driver to guarantee a stable voltage. Also, an error amplifier minimizes the difference between the actual output and the desired output value. The input filter is shown in Figure 6.

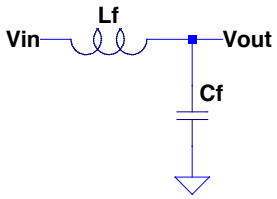

Figure 6. Input filter.

R_f has been introduced in order to get rid of oscillations near the resonance frequency. The R_f value is optimized by setting a damping factor higher than the critical damping value for the filter. This is done to assure that we will not have any overpeaks. This condition can be obtained to be:

$$R_f \leq \frac{1}{2} \cdot \sqrt{\frac{L_f}{C_f}} \qquad (3)$$

For the value of L_f and C_f taken in our design, we have taken a value of R_f of 11 Ω in order to have a safety margin. The output driver is based on three bipolar transistors. The circuit can be seen in Figure 7.

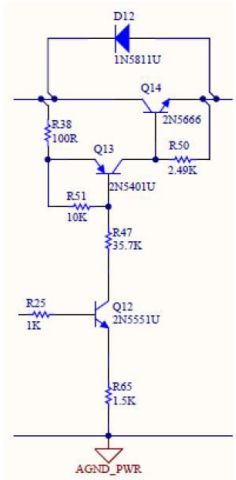

Figure 7. Output driver schematics.

One of the main design points consists in limiting the current at the input of the driver, coming from the error amplifier. A too high current could end up with the destruction of the input transistor. This limitation has been overcome by a proper election of two resistors of the output driver, R25 and R65, taking into account the maximum value of the input voltage coming from the error amplifier. Taking a maximum load current of 30 mA and fixing a value of R25 to 1 kΩ, we can obtain R65 with the following expression:

$$R65 = \frac{V_{O\max} - 0.7V - I_B(Q12) \cdot R25}{I_C(Q12)} \cong 2.8k\Omega \qquad (4)$$

Additionally, we have to verify the Safe Operation Area of the output transistor. For our transistor, this can be observed in the corresponding figure provided by the manufacturer. As it is sure that our transistor current will always be under 90 mA and that the output voltage will never reach a value of 70V, we can be sure to be always on the safe area.

4.2 Dual TT driver

It consists of two components: a Digital-to-Analog converter (DAC) for obtaining the required voltage, and amplifiers for adapting this voltage to the input levels demanded by the piezoelectric load. The design is shown in Figure 8.

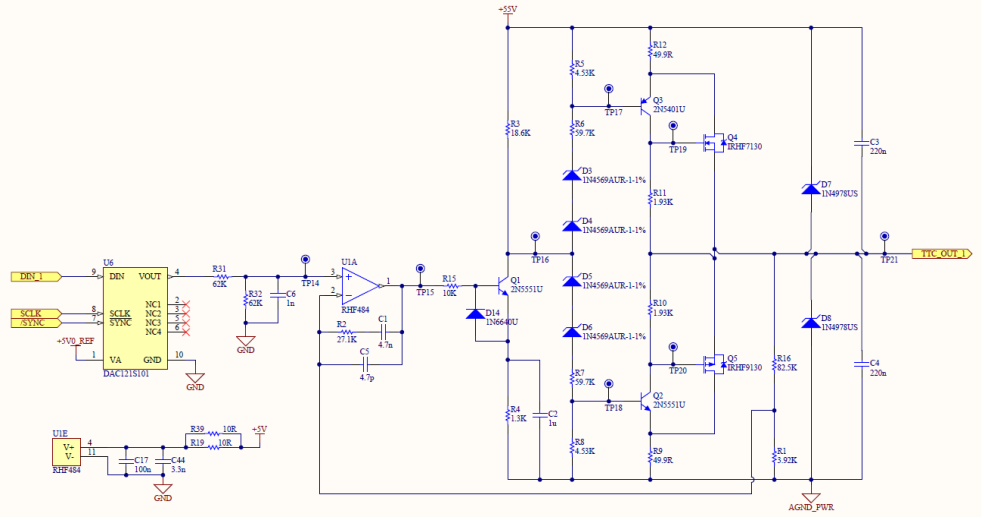

Figure 8. TT Driver schematics.

The amplifiers are based on a transconductance amplifier architecture. It can be divided in three stages:

- Input stage: Adapts the input signal to values required by the driver.
- Control stage: Generates the output signal from the input command.
- Output stage: Generates the needed current values at the generated output voltages.

At the input stage, we define the values of the resistances at the Zener diodes branch by selecting the desired Zener diode operating current and setting the base-emitter voltage (V_{be}) of the transistor to be near its maximum value at the quiescent state. The use of Zener diodes allows larger current variations through this branch. The expression for obtaining these resistances is:

$$R5 + R6 = R7 + R8 = \frac{55V - 4 \cdot I_Z}{2 \cdot I_{R5}} \cong 66.1k\Omega \quad (5)$$

The control stage minimizes the error between the actual output voltage value and the commanded output voltage from the input. The feedback voltage divider resistors are obtained by the gain factor of the desired output with respect to the input.

The output stage is based on two current mirrors. The output transistors will be cut or completely open. In order to guarantee that they can provide the maximum current, the upper and lower resistor can be set properly:

$$R9 = R12 = \frac{V_{BE\max}}{I_L} = \frac{1V}{19.5mA} \cong 50\Omega \quad (6)$$

Finally, the two resistors connected at the output can be defined taking into account the threshold voltage of the MOS transistors and assuming a small current through the bipolar transistors:

$$R10 = R11 = \frac{V_{th}}{I_e} = \frac{3V}{1mA} \cong 3k\Omega \quad (7)$$

5. SYSTEM CONTROL

The whole system is controlled by an FPGA based on a Xilinx Virtex 4 architecture. An analysis of stability has shown that low latency is required in order to ensure the desired stability. For this reason, a fully parallelized solution has been implemented using a Squared Differences (SD) algorithm. The output of the SD is fed to a parabolloid interpolation module, that determines the position of the minimum with a precision over 1/8th of a pixel.

6. RESULTS

Results show that the full system reaches an attenuation of 1/10th of a pixel at 10Hz, which is the scientific requirement. Experimental results for the TTC show a good performance of this stage, providing a high voltage span, enough slew-rate and the needed stability levels. More detailed analysis of these results can be found in a contributed paper in the same conference[8]. One of these results is shown in Figure 9, just as a representative result, where we can observe one of the simulated images obtained by the CTC.

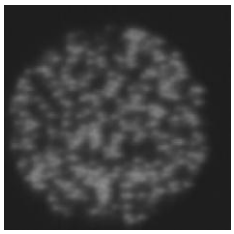

Figure 9. Simulated sun image obtained by the CTC.

ACKNOWLEDGMENTS

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