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Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *February 15, 2024*
Published: *April 9, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

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https://doi.org/10.1088/1748-0221/19/04/C04020

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Abstract: The Belle II collaboration has initiated a program to upgrade its detector in order to address the challenges set by the increase of the SuperKEKB collider luminosity, targeting 6×10^{35} cm^2 s^{-1}. A monolithic CMOS pixel sensor named OBELIX (Optimized BELle II pIXel) is proposed to equip 5 detection layers upgrading the current vertex detector. Based on the existing TJ-Monopix2, OBELIX is currently designed in 180 nm CMOS process.

Keywords: Digital electronic circuits; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout; Radiation-hard electronics

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Contents

1 Requirements for a pixel sensor at Belle II

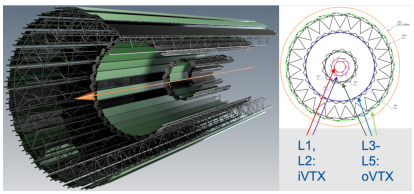

Figure 1. CAD 3D view and 2D cut of 5 VTX detectors layers.

Belle II is a super B-factory experiment studying tau, charm and beauty physics at the asymmetric 7 GeV electron- 4 GeV positron SuperKEKB collider located in Tsukuba, Japan [1]. First data were recorded in Spring 2018 [2]. The collider reached the world luminosity record of $4.7{\times}10^{34}$ cm^{-2} s^{-1} in June 2022, with a next target of $6{\times}10^{35}$ cm^{-2} s^{-1}. To do so, an upgrade of the detector's interaction region is considered during a long shutdown foreseen around 2028. Extrapolation of current beam-induced background at the target luminosity predicts that the current Vertex Detector (VXD) could reach its occupancy limit, depending on the necessary safety factor assumed to cover the large uncertainty associated to the extrapolation 3 % [3]. To cope with large beam-induced background levels, a new vertex detector concept called VTX is proposed (figure 1). It consists of 5 detection layers covering radii from 1.4 cm to 14 cm with an angular acceptance from 17 to 160 degrees. All layers are equipped with a thin, radiation-hard and fully depleted monolithic active pixel sensor called OBELIX. This sensor inherits the design of the TJ-Monopix2 chip with modifications allowing to meet the requirements listed in table 1.

Table 1. Belle II VTX requirements from simulations.

From simulations	Belle II VTX
Spatial resolution.	$<$ 10–15 µm
Total material buget (Inner-outer) layers	0.1–0.8 %X0
Max hit rate	120 MHz/cm^2
Time precision	$<$ 100 ns
Trigger freq & delay	30 kHz & 5–10 µs
Rad. hard TID	$<$ 100 kGy/year
Rad. hard fluence	$<$ $50{\times}10^{12}$ n_{eq}cm^{-2}/year
Power	$<$ 200 mW/cm^2

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2 TJ-Monopix2

The TJ-Monopix2 [6, 9], is a depleted monolithic active pixel sensor (DMAPS) based on the column-drain architecture and manufactured in 180 nm CMOS imaging process by Tower Semiconductor. A low dose deep n implant is added under the pixel matrix to enhance radiation tolerance [4]. It is the last prototype of the TJ-Monopix series originally developed for the ATLAS Inner Tracker upgrade [5–7]. The overall size of the sensor is 2×2 cm^2 including an active area of 16.9×16.9 mm^2 with a 512×512 matrix of 33.04×33.04 μm^2 pixels. The pixel analog front-end is an evolution of the one implemented in ALPIDE sensor [8], optimized for fast timing applications. The pixel matrix includes four pixel flavours based on the front-end amplifier variety and detector input coupling (AC or DC) configuration. The sensor records the timing information of the incoming particle thanks to 7 bit Leading Edge (LE) and 7 bit Falling Edge (FE) at 25 ns timestamp. There are 3 bit per pixel, allowing each pixel threshold to be tuned individually. With the column-drain architecture [11, 12], all the data (address, LE & TE), Beam Crossing ID (BCID) clocks and control signals (read, freeze, token) are transmitted to and from the bottom peripheral along each double column. The sensor can handle a hit rate higher than 120 MHz/cm^2. The prototype was submitted in Q4 2020 and returned from fabrication in Q1 2021. Various laboratory measurements and test beams demonstrated that the performance of the TJ-Monopix2 pixel matrix satisfies the VTX requirements with a detection efficiency around 99.8 % at an average threshold of 200 e- and threshold spread of less than 20 e- [9].

3 The OBELIX design

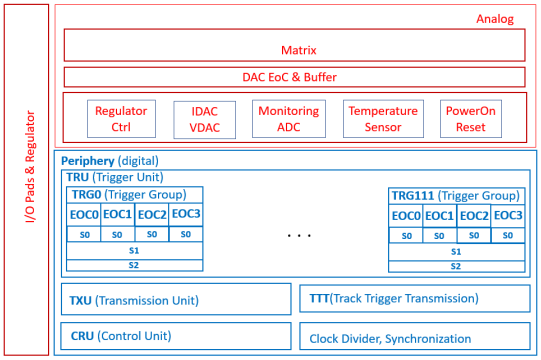

Figure 2. Funtional description of OBELIX.

The OBELIX sensor inherits the performance of the pixel matrix and analog steering blocks from TJ-Monopix2 sensor. The main design effort focuses on chip level integration to increase the active area from 16.9×16.9 mm^2 to 15.3×29.6 mm^2 and to develop a new digital processing circuit handling the hit and trigger rate required by Belle II. An on-chip regulator is also being developed in OBELIX to compensate for the voltage drop along the ladder and thus minimising the material budget dedicated to power distribution at the system level. The whole design also satisfies the VTX constraint for a total power dissipation under 200 mW/cm^2.

The overall dimensions of the OBELIX sensor are 18812 µm in height by 30168 µm in width including 464×896 pixels of 33.04×33.04 μm^2 (figure 2). In top of the position, the timing information of the incoming hit is recorded through 7 bit Leading Edge (LE) and Falling Edge (FE) of 50 ns (possibly 100 ns) timestamp instead of 25 ns in TJ-Monopix2. This information is also used to store the pixel signal with the time over threshold (ToT). OBELIX also features new and optional functionalities. They include in the analog domain: a monitoring 10-bit ADC, a power-on reset and a temperature sensor, and in the digital domain: a peripheral high resolution time stamping and a fast coarse granularity hit information as trigger input.

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3.1 The Digital on Top (DoT) integration flow

In order to save development time, we adopt the Digital on Top (DoT) flow to realize the integration of OBELIX sensor. This flow offers a flexible floorplan and a powerful tool to analyse early the power distribution of the circuit, which is crucial for large circuit design and allows us to adapt efficiently TJ-Monopix2 design. In order to share tasks between the different design teams, we use the hierarchical flow using top-down methodologies. First, we import the design from its verilog description into the environment of Innovus Implementation System (Innovus).

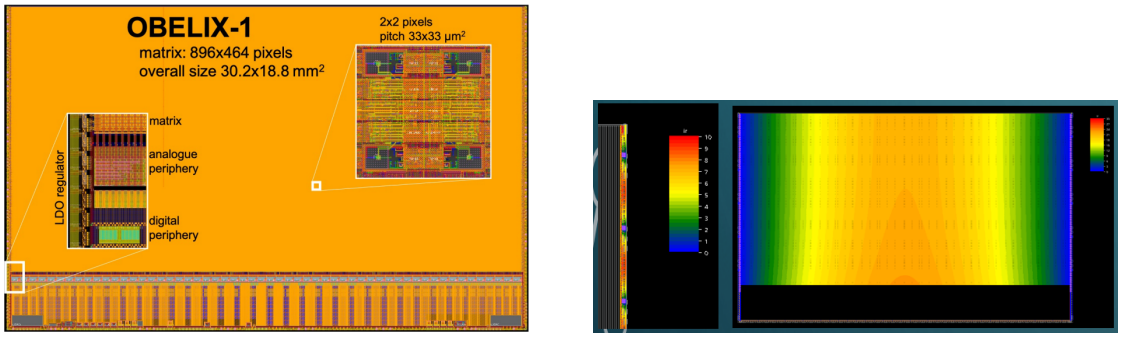

Figure 3. OBELIX floorplan and IR drop simulation of the matrix without regulator.

At the beginning, all the blocks are considered as "blackbox", which is an empty module that we can assign a dimension. Once we have attributed pin and partition to those blocks, they are transformed into "hard blocks". In the case of OBELIX, different analog macro-modules with finished layout can already replace their respective blackbox. As the TJ-Monopix2 has been designed using Analog on Top (AoT) flow, we have to re-adapt some layouts in order to make them modular. For example, in one double column (DC) of the pixel matrix, the digital bus is shared between the left and right column, and is therefore independent from one DC to the other. However, in order to optimise the area, the analog bias is shared between two DCs. In the TJ-Monopix2, the layout of two adjacent DCs overlap, which is not convenient for the DoT flow. In the modified layout, each DC is independent so that we can easily integrate them in Innovus environment. This modification also affects the DAC End of Column (DAC_EoC) which is placed at the bottom of the matrix and allows to buffer the bias signals. As for digital part, in terms of integration, we treat them as a unique blackbox at top level.

The next step is to elaborate the floorplan by placing various blackbox and macro-modules to optimise the data path and so minimise further routing congestion. This step is followed by the definition of the power plan so that we can perform the power analysis to estimate the consistency of the power distribution (figure 3). Once the initial power plan is complete, we assign the I/O pins position to various blackboxes. In our case, we align the digital to the analog pins because most of them are well defined. From now on, we split the design into partitions by propagating the I/O pins and power constraints to each blackbox, and the corresponding design teams can work on their partition. The latter is considered as an intermediate block between a blackbox and a macro module. At the top level, we run the global routing to connect different blocks together and when all the sub-blocks are finished, we replace them with their macro-module and proceed with global verifications.

3.2 Analog design

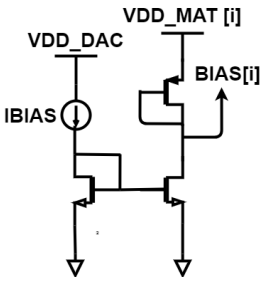

Figure 4. Supply voltage drop compensation concept.

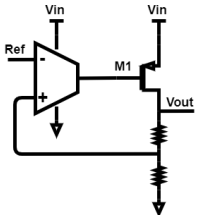

Figure 5. Low Dropout Regulator synopsis.

The sensor has additional features compared to TJ-Monopix2, such as a monitoring 10-bit ADC, power-on-reset, temperature sensor and on-chip regulation, even though most of the circuitry has been reused. Power distribution is a major concern as OBELIX is larger than TJ-Monopix2 and leads to performance degradation. The strategy adopted in TJ-Monopix2 and OBELIX is to power the matrix from both sides using the top metal level (Metal 6). At the bottom, the DAC_EoC buffer replicates the power voltage of each double column and readjusts its bias current so that it remains unchanged from one DC to the other. Figure 4 illustrates the concept of power drop voltage compensation by probing the power voltage of column i (VDD_MAT[i]) and readjusting its bias current (BIAS[i]).

The voltage drop from one row to the other cannot be exactly compensated but is minimised with the following strategy. Two LDOs (figure 5), are implemented to supply the matrix from both sides through their pass transistor M1. This is stretched along the matrix to minimise the non-active area and distribute the current evenly. There are five groups of power pads per side, consisting in an unregulated input voltage Vin from 2 V to 3 V, a 1.8 V regulated Vout for external coupling purposes and a ground pad. The distributed pass-transistor also helps to reduce the voltage drop along the matrix.

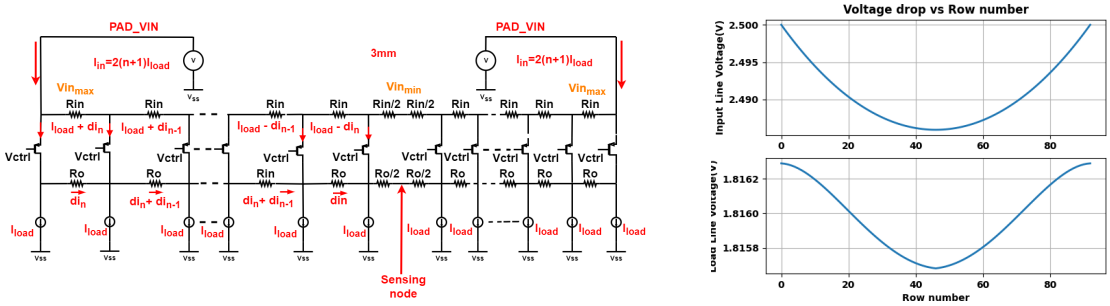

Figure 6. Current distribution across the resistance network and simulation result of voltage drop across 92 pixel rows.

As explained in figure 6, suppose we have two unregulated voltages Vin placed at a certain distance from each orther. The 1.8 V output voltage is regulated at a chosen point which could be set in the middle of the line. Each distributed pass transistor will drive the current from the Vin line (input line) to the load line. The voltage drop on the input line is due to the total current flow from the Vin to the centre of the line which is much higher than the voltage drop on the load line. This depends on the accumulation of the difference between the current driven by the pass-transistor and the load current. In our case, the matrix is powered by 5 groups of power pads. The distance between two input power pads is approximately 3 mm. The voltage drop across the power line is simulated with 1.66 Ω/mm input line, 2.87 Ω/mm load line, 2.5 V input voltage and 23 mA load current. The latter corresponds to the power consumption of 92 pixel rows, as the matrix is powered from both sides and is divided into 5 power input groups. Thanks to the distributed pass transistor, the result in figure 6 shows that

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even with a load line that is more resistive than the input line, the input drop voltage is reduced from ~14 mV to ~600 µV. This preliminary result allows to choose the number of power groups and the width of the power distribution line. The strategy will be fully validated after running the IR drop for the entire circuit, including the matrix and the regulator, whose design is under finalisation.

3.3 Digital design

The new digital processing consists of five functional blocks [10]: Trigger Unit (TRU), Transmission Unit (TXU), Synchronisation Unit (SRU), Control Unit (CRU) and the Track Trigger Transmission (TTT). The TRU (figure 7) implementation allows to handle a maximum hit rate of 120 MHz/cm^2 with a 30 kHz trigger rate and 10 µs trigger latency. Data from 4 double columns are merged via a round-robin arbiter before being sent to a two-stage buffer. As the matrix releases the data at the trailing edge of the signal (TE), the hit data arrives at the periphery in random order. The first stage of the buffer is a FIFO and acts as a pre-memory whose size allows to hold the event information for most of the trigger latency time. The second stage is the main trigger memory, where the logic associates hit data and trigger information before being sent to the TXU. The TXU frames the data with 8b/10b encoding and sends it to the 320 MHz serial LVDS output.

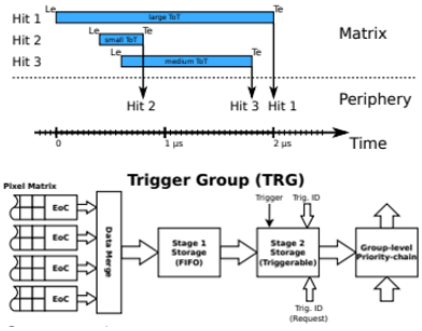

Figure 7. Trigger Unit Synopsis.

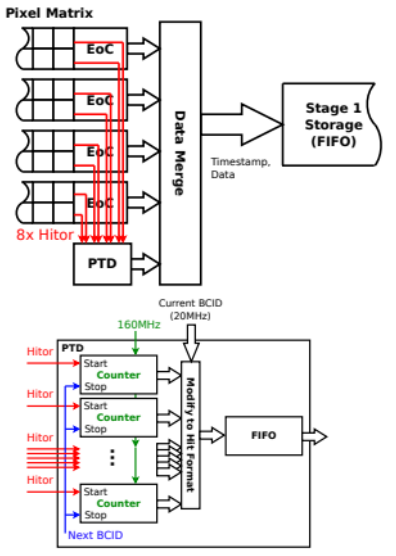

Figure 8. Peripheral Time to Digital (PTD) converter.

The SRU and CRU ensure control and configuration of various sensors parameters. They both are similar to the TJ-Monopix2 blocks, which is a modified version of the decoder used in the RD53A [6, 13]. The TTT can provide a coarse but fast (~10 ns resolution with 3 layers) hit information to Belle-II trigger system by considering the whole matrix as 2 to 8 logical macro pixels. An additional feature of OBELIX is the Peripheral Time to Digital (PTD) converter (figure 8), which, thanks to the 160 MHz input clock, converts the hit arrival time of a logical macro-pixel into digital value and so offer a higher resolution (~6 ns) than the 50 ns that provide the in-pixel timing information. However, this function is very power hungry and is not suitable for the high hit rate of the two internal layers L1 & L2.

4 Conclusion

This paper describes a new CMOS pixel sensor called OBELIX proposed to upgrade the Belle II vertex detector. The first version, OBELIX-1, is expected to be submitted at the beginning of 2024. Based on the design of TJ-Monopix2, the chip offers a larger active area, on-chip power regulation and a new digital processing capable of handling the hit and trigger rates suitable to operate Belle II at a peak luminosity of 6×10^{35} cm^{-2} s^{-1}. The DoT flow used for top integration is also shown to optimise the development time and increase circuit reusability in the context of a multi-team design effort.

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Acknowledgments

This work has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreements no 101004761 (AIDAinnova), was supported by Grant CIDEGENT/2018/020 of Generalitat Valenciana (Spain) and has been published under the framework of the IdEX University of Strasbourg. The authors thank Yavuz Degerli (CEA-IRFU) for the authorisation to use his power-on-reset block.

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