Conduction mechanisms and charge storage in Si-nanocrystals metal-oxide-semiconductor memory devices studied with conducting atomic force microscopy

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In this work, we demonstrate that conductive atomic force microscopy (C-AFM) is a very powerful tool to investigate, at the nanoscale, metal-oxide-semiconductor structures with silicon nanocrystals (Si-nc) embedded in the gate oxide as memory devices. The high lateral resolution of this technique allows us to study extremely small areas ($\sim$300 nm^2) and, therefore, the electrical properties of a reduced number of Si-nc. C-AFM experiments have demonstrated that Si-nc enhance the gate oxide electrical conduction due to trap-assisted tunneling. On the other hand, Si-nc can act as trapping centers. The amount of charge stored in Si-nc has been estimated through the change induced in the barrier height measured from the *I-V* characteristics. The results show that only $\sim$20% of the Si-nc are charged, demonstrating that the electrical behavior at the nanoscale is consistent with the macroscopic characterization. © *2005 American Institute of Physics*. [DOI: 10.1063/1.2010626]

Memory devices based on metal-oxide-semiconductor (MOS) structures with Si nanocrystals (Si-nc) embedded in the gate oxide[1–5] show many advantages compared to the current floating gate technologies. In particular, they offer fast writing speeds at smaller injection voltages, extremely small degradation, smaller lateral leakage currents, and, therefore, longer retention times. These developments in nanoscale silicon electronics, however, require tools to locally characterize the electrical properties of the Si-nc. In this direction, conductive atomic force microscopy[6–8] (C-AFM) has been recently used to estimate from topographical images the amount of charge stored in Si-nc deposited on different substrates.[9,10] However, few works have been devoted to investigate the electrical properties of MOS-based memory devices with embedded Si-nc at the nanoscale. In this work, a C-AFM has been used to study the conduction mechanisms of SiO_2 gate oxides with Si-nc as storage nodes. The amount of charge stored in few Si-nc has also been estimated from electrical measurements.

MOS structures with a SiO_2 thickness, t_{ox}, of 23 nm [obtained from transmission electron microscopy (TEM) images] thermally grown on a *p*-type Si substrate and with a polysilicon gate have been analyzed. In some of them, the gate oxide was implanted with 15-keV Si^+ ions with a dose of 2×10^{16} cm^{-2}.[2] The peak concentration was estimated by simulation to be of about 10 at. % at a depth of $\sim$22 nm with a width at half maximum of the ion implantation distribution within the oxide of $\sim$9 nm. The rest were used as a measurement reference. After removing the polysilicon gate,[8] when working on bare oxides, the conductive tip of the C-AFM plays the role of the gate electrode. Therefore, MOS structures of only $\sim$300 nm^2 can be analyzed.[8] The gate oxides (with and without Si-nc) were electrically characterized by measuring current-voltage (*I-V*) characteristics, obtained when a ramped voltage test (RVS), which consists of a forward followed by a backward voltage ramp, is applied at a fixed location of the oxide.

To begin with, the electrical conduction of MOS structures without Si-nc has been investigated and will be considered as reference. Figure 1(a) (squares) shows a typical forward *I-V* characteristic obtained on a fresh oxide. Two different conduction regimes are observed with a transition at $\sim$25.5 V. For high voltages, the *I-V* curve can be fitted to the

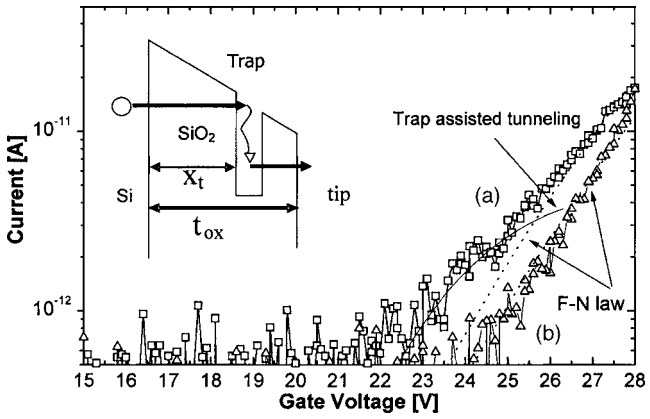

FIG. 1. Forward (a) and backward (b) *I-V* characteristics (symbols) measured on a fixed location of a gate oxide (t_{ox}=23 nm) without Si-nc. For voltages larger than $\sim$25.5 V, both curves have been fitted to the FN law (dashed line) using different ϕ. The leakage current observed in the forward ramp (fresh oxide) for voltages below $\sim$25.5 V has been fitted to the model proposed by Kamohara *et al.*, which attributes the excess of current to trap-assisted tunneling through single defects in the oxide. A schematics showing this conduction mechanism is shown in the inset.

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Fowler-Nordheim (FN) law[11] [Fig. 1(a), dashed line],

$$I = A_{\text{eff}} \frac{q^2 m_0}{8\pi h m_{\text{ox}}^* \Phi} \frac{V_{\text{ox}}^2}{t_{\text{ox}}^2} \exp\left(- \frac{8\pi\sqrt{2qm_{\text{ox}}^*} t_{\text{ox}} \Phi^{3/2}}{3hV_{\text{ox}}} \right), \quad (1)$$

being V_{ox} the oxide voltage, q, the electron charge, h, Planck's constant, $m_{\text{ox}}/m_0=0.5$ the effective mass of electrons in the SiO_2 conduction band,[6] ϕ, the injection barrier height, and A_{eff} the effective emission area at the injecting electrode [~ 300 nm^2 (Ref. 8)]. By considering $t_{\text{ox}}=23$ nm, ϕ was found to be 2.73 eV. For voltages below ~ 25.5 V, the current is slightly larger than that expected for the FN conduction. To investigate the excess of current, we have considered that it could be attributed to one-trap-assisted tunneling (TAT) through defects in the oxide (Fig. 1, inset). Taking into account this consideration, the measured *I-V* curve has been fitted to the model proposed in Ref. 12 which estimates, from Eq. (2), the stress-induced leakage current that flows through the traps generated during the electrical stress,

$$I = K \exp\left(- \frac{4}{3} \frac{\sqrt{2m_{\text{ox}}}}{h} \frac{1}{qE_{\text{ox}}} \right) \times (E_t^{3/2} - [E_t - qE_{\text{ox}}(t_{\text{ox}} - x_t)]^{3/2}), \quad (2)$$

being K a constant that includes the trap density and the area of injection, E_{ox} the field oxide, E_t, the trap energy, and x_t, the distance of the trap to the injecting electrode. A good fit to this model [Fig. 1(a), continuous line] was obtained when $K=1.35\times10^{-3}$ A, $E_t=5.9$ eV, and $x_t=18$ nm, indicating that traps are near the tip-sample interface. Although the origin of these traps is not clear (further studies, which are out of the scope of this work, should be performed to clarify this point), they could be related to native or sample deprocessing defects. These defects will be considered when analyzing MOS structures with Si-nc.

The electrical conduction through reference oxides after being subjected to an electrical stress has also been studied. Figure 1(b) (triangles) shows the backward *I-V* characteristic measured at the same oxide location where curve (a) was obtained. The low-field leakage current in curve (a) is no longer registered, which points out that the defects that lead to that leakage current are deactivated after the first RVS and only are important during the initial transient. A shift of the *I-V* curve to larger voltages is observed. This behavior can be attributed to negative charge trapping in the defects created during the forward RVS,[13] leading to an increase of ϕ and, therefore, to a decrease of the oxide conductivity. The backward *I-V* curve has been fitted to the FN law (dashed line) and ϕ was found to be 2.78 eV. The shift observed in ϕ can be used to estimate the amount of charge trapped during the stress.[14] By considering that the defects are concentrated near the interface of the injecting electrode,[15] a charge density of $\sim 0.1\times10^{-7}$ C/cm^2 is determined, which corresponds to $\sim 1-2$ electrons under the C-AFM tip (~ 300 nm^2). Note that the trapped charge due to the oxide degradation is, as expected, smaller than that detected after the oxide breakdown (~ 30 electrons).[8]

Identical gate oxides with implanted Si-nc have also been investigated. Figure 2(a) (squares) shows a typical forward *I-V* curve on a fresh Si-nc embedded structure. Two

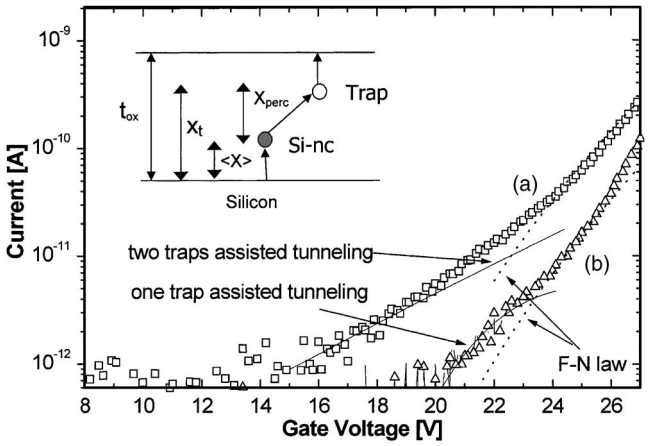

FIG. 2. Forward (a) and backward (b) *I-V* characteristics (symbols) measured on a fixed location of a gate oxide ($t_{\text{ox}}=23$ nm) with embedded Si-nc. For voltages larger than ~ 23 V, both curves have been fitted to the FN law (dashed line) using different ϕ. The leakage current observed in the *I-V* curves for voltages below ~ 23 V has been fitted to the model proposed by Kamohara *et al.* (a) and Degraeve *et al.* (b), which attribute, respectively, the excess of current to trap-assisted tunneling through single and two trap paths. A schematics showing the conduction mechanism through a two-trap percolation path is also shown in the figure (inset).

conduction regimes are again observed with a transition at ~ 23 V. For high voltages, the current injection is of the FN type with $\phi \sim 2.40$ eV [Fig. 2(a), dashed line]. This value is lower than that obtained in the MOS structures without Si-nc. The larger conductivity in this voltage range could be associated to a tunneling current assisted by Si-nc and/or other defects in the oxide, like those generated during ion implantation.[16,17] However, since the ion implantation was followed by thermal annealing, which leads to the Si precipitation and synthesis of Si-nc with a well-passivated Si/SiO_2 interfaces,[18] the implanted induced damage completely disappears after the annealing step, as it was monitored by the photoluminescence peaks related to defects in the SiO_2 matrix.[19] Therefore, the leakage current can only be attributed to TAT through Si-nc.

For low voltages (from ~ 15 to 23 V), leakage currents superimposed to the FN regime are observed. This leakage current is about one order of magnitude larger than that registered in reference oxides, suggesting that the conduction mechanism could be different. To interpret its origin, we have considered the model proposed in Ref. 20 which explains the current observed in SiO_2 gate oxides after stress, before breakdown. In Ref. 20 it was demonstrated that, due to the electrical stress, the leakage current can be explained in terms of TAT through a percolation path defined by the alignment of two traps (Fig. 2 inset) that connects both electrodes, which drives a current determined by the maximum of the trap-trap or trap-interface distance (x_{perc}). A two-trap-assisted tunneling has also been used to explain the anomalous leakage current in flash memories.[20] Assuming that Si-nc can act as trapping sites and that, as in the case of the reference oxides, defects are present near the tip-sample interface, this model can explain the leakage current registered in fresh gate oxides with Si-nc at low voltages. To show this point, we have fitted the low-field *I-V* characteristic of Fig. 2(a) (squares) to the percolation model[20]

$$I_{\mathrm{perc}} = A \exp\left(\frac{B}{x_{\mathrm{perc}}}\right), \tag{3}$$

being A and B linear functions of the oxide field. In our case, x_{perc} has been defined as the difference between the Si-nc position, $\langle x \rangle$, and the defects observed in reference oxides, x_t (Fig. 2 inset). A good fit was obtained for $x_{\mathrm{perc}} \sim 9.5$ nm [Fig. 2(a), continuous line]. Since $x_t = 18$ nm (obtained from the fresh data in Fig. 1), $\langle x \rangle$ was estimated to be ~ 8.5 nm. This result is compatible with the distribution of Si-nc within the oxide (TEM images have shown that Si-nc are located between 3.5 and 10.5 nm from the channel). The good agreement of the fitting to the experimental data suggests that the dominant conduction mechanism (for low voltages) when Si-nc are present in the oxide is TAT through two sites percolation path (Si-nc and defects) instead of TAT through single defects. The electrical conduction of MOS structures with Si-nc after a RVS has also been investigated. Figure 2(b) (triangles) shows the backward *I-V* characteristic measured at the location where Fig. 2(a) was obtained. A shift to larger voltages and an excess of current at voltages below 23 V are observed. The enhanced conduction at $V_G < 23$ V has been fitted to Eq. (2), which corresponds to TAT through one trap path [Fig. 2(b), continuous line], and x_t was found to be 4.8 nm. This result suggests that, due to the proximity of the trap sites location to the injecting interface, the leakage current observed in Fig. 2(b) could be attributed to single TAT through the Si-nc and that, as for reference samples, the defects close to the tip interface have been masked or deactivated. For $V_G > 23$ V, the *I-V* curve has been fitted to the FN law with ϕ being 2.55 eV. Now, the shift observed in ϕ is higher than in reference samples, suggesting an excess of charge in the oxide of the implanted samples. In particular, for the gate oxide location studied in Fig. 2, this excess was estimated to be $\sim 2-3$ electrons. Inferred from an implantation fluency of 2×10^{16} cm^{-2} and a mean Si-nc size of 3 nm (measured by TEM), the density of Si-nc is $\sim 6.3 \times 10^{12}$ cm^{-2} (~ 10 Si-nc in ~ 300 nm^2). By assuming that the shift observed in ϕ can be related to electrons stored in the Si-nc, the occupation level of the nanocrystals is $\sim 20\%$, in agreement with data obtained from macroscopic measurements.[3]

To sum up, the conduction mechanisms and charge storage in MOS devices with Si-nc as memory devices have been investigated with C-AFM. A transient leakage current is observed in the first low-field *I-V* curves of both reference and implanted oxides, which has been related to TAT through some undetermined defects. The results demonstrate that Si-nc can act as trap sites and that they enhance the electrical conduction due to TAT. The change in ϕ at the injecting electrode has been used to estimate the amount of charge stored in the Si-nc. The results show that only $\sim 20\%$ of the Si-nc are charged. In conclusion, this paper demonstrates the capability of the C-AFM to perform a nanoscale analysis of the electrical properties of the Si-nc and, therefore, to investigate in detail the performance of MOS structures with Si-nc as memory devices.

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