Stability of hydrogenated nanocrystalline silicon thin-film transistors

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ABSTRACT

Hydrogenated nanocrystalline silicon thin-films were obtained by Catalytic Chemical Vapour Deposition at low substrate temperatures (150 ºC) and high deposition rates (10 Å/s). These films, with crystalline fractions over 90%, were incorporated as the active layers of bottom-gate thin-film transistors. The initial field-effect mobilities of these devices were over 0.5 $cm^2/V{\cdot}s$ and the threshold voltages lower than 4 V. In this work, we report on the enhanced stability of these devices under prolonged times of gate bias stress compared to amorphous silicon thin-film transistors. Hence, they are promising candidates to be considered in the future for applications such as flat-panel displays.

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) are widely used as the active elements in large-matrix liquid crystal displays [1]. Unfortunately, these devices show undesired threshold voltage shifts after prolonged bias stress applied to the gate electrode. The cause of this instability has been attributed to either charge trapping in the gate insulator or defect creation in the band gap of the a-Si:H active layer [2]. In the case of high quality gate insulators, the degradation of the semiconductor active layer is the factor which determines the stability of the device.

Traditionally, a-Si:H TFTs are obtained by Plasma Enhanced Chemival Vapour Deposition (PECVD) at moderate substrate temperatures (<300 ºC). The Catalytic Chemical Vapour Deposition (Cat-CVD) has recently arisen as an alternative technique to obtain a-Si:H and also hydrogenated nanocrystalline silicon (nc-Si:H) at distinctly higher deposition rates. Furthermore, a Cat-CVD set-up is easier to handle, and the implementation and upkeep costs are much lower than for a PECVD one.

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In this paper, we report on the stability of nc-Si:H TFTs deposited at indeed low substrate temperatures (150 ºC) by Cat-CVD. These devices were degraded by applying a gate bias stress for a prolonged time.

2. Experimental

The nc-Si:H TFTs studied in this work were inverted-staggered structures consisting of an undoped nc-Si:H active layer (200 nm) deposited by Cat-CVD on a thermally-grown silicon dioxide (250 nm) on n-type (1-10 Ω·cm) silicon wafers (100) as shown in Fig. 1. The top nc-Si:H n^+-doped layer (50 nm) to contact the drain and source contacts was also deposited by Cat-CVD. Additionally, a chromiun layer was thermally evaporated to define the metallic contacts by photolithography and dry-etching. The aspect ratio of the TFTs was 5, corresponding to a channel width W = 50 μm and length L = 10 μm.

The undoped nc-Si:H active layer of these devices was obtained by Cat-CVD in an ultra high vacuum set-up, with a base pressure lower than 10^{-8} mbar, described elsewhere[3]. The tungsten wire of 0.5 mm diameter was heated to 1700ºC to catalytically decompose the gas mixture consisting of 4 standard cubic centimeters (sccm) of silane diluted into 76 sccm of hydrogen. In order to obtain the n^+-doped layer, 2 sccm of phosphine were added to the base gas mixture. The process pressure was fixed around 10^{-2} mbar by means of a butterfly valve between the deposition chamber and the turbomolecular pump (360 l/s). The substrate temperature was around 150 ºC.

The TFTs were measured in the dark and under vacuum conditions. Their stability was investigated by the application of a gate bias stress of 30 V at two different temperatures (25 ºC and 60 ºC) for several days. The TFT electrical characteristics were measured by means of a semiconductor parameter analyser (HP4145B) and a programmable temperature controller (MMR K-20).

3. Results

The selected deposition conditions described in the previous section enabled nc-Si:H samples to be obtained with crystalline fractions over 90%, as deduced by Raman spectroscopy. X-ray diffraction spectra showed a (111) crystalline preferential growth. The hydrogen content calculated from the Si-H wagging band in the infrared transmittance spectrum was around 4%[4]. Regarding the electrical properties, the undoped samples used as the active layers of the TFTs showed room temperature dark

conductivities on the order of 10^{-6} $\Omega^{-1}cm^{-1}$, with thermal activation energies around 0.5 eV. The density of deep states (dangling bonds) in the band gap was estimated to be less than 10^{16} cm^{-3} by Photothermal Deflection Spectrometry (PDS). The n^+-doped layers showed room temperature dark conductivities on the order of a few $\Omega^{-1}cm^{-1}$, with thermal activation energies lower than 100 meV.

The initial output characteristics of the devices are shown in figure 2. Neither significant current crowding near the origin nor the kink effect for high drain-source voltages was observed. These results indicate a low contact resistance at the electrodes without important carrier injection for higher drain-source voltages. Additionally, a good saturation of the output characteristic is observed for all the gate-source voltages applied.

Figure 3 shows the saturation characteristics ($V_{ds}=V_{gs}$) of one of the TFTs after different stress times. These curves could be fitted according to equation (1) in order to calculate both the field-effect mobility (μ_s) and threshold voltage (V_{th}) for increasing stages of degradation.

$$I_{ds} = \frac{1}{2}\frac{W}{L}\mu_s C_{ox}\left(V_{gs} - V_{th}\right)^2 \qquad (1)$$

The calculated values are shown in figure 4, where the decrease of the field-effect mobility and the absolute threshold voltage shift are plotted as a function of the stress time. The initial threshold voltage was only 3.4 V, which increased up to 7.9 V after 44 hours with a 30 V bias applied to the gate electrode at 60 ºC. The saturation mobility slightly degraded from the initial value of 0.56 $cm^2/V{\cdot}s$ to 0.40 $cm^2/V{\cdot}s$ after degradation.

Despite the high crystalline fraction of the nc-Si:H layer incorporated in the device, the calculated values of mobility and threshold voltage are quite similar to those typically obtained in a-Si:H TFTs. However, the mobility degradation and the threshold voltage shift are significantly lower than in a-Si:H TFTs. Devices showing stabilities comparable to the present results have been also obtained by Cat-CVD, but these TFT's were grown at much higher substrate temperatures (> 450 ºC) [5]. Actually, in order to compare the stability of TFTs with different initial threshold voltages, the relative threshold voltage shift is used, and is defined as follows

$$\Delta V_{th}^{rel} = \frac{V_{th} - V_{th}^{ini}}{V_{bias} - V_{th}^{ini}} \qquad (2)$$

with V_{bias} the gate bias applied and V_{th}^{ini} the initial threshold voltage.

Figure 5 shows the dependence of the relative threshold voltage shift on the gate bias stress time for two TFTs obtained under the same deposition conditions but degraded at different temperatures. A faster degradation is observed for devices degraded at a higher temperature. Nevertheless, the ΔV_{th}^{rel} values so obtained were moderate and comparable to ones reported for devices deposited at higher substrate temperatures [5].

4. Discussion

Structural characterizations on nc-Si:H layers, obtained under the same deposition conditions as those used for devices, exhibited a crystalline fraction over 90%. However, the low field-effect mobility in the TFTs, together with the saturated sheet conductance activation energy (≥0.15 eV) obtained for high applied gate-source voltages [6], would indicate that the conductive channel forms in the initial incubation layer with a lower crystalline fraction.

Several microscopic models could explain the metastability of the TFTs. A stretched-exponential behaviour, similar to that typically found for defect creation, could be explained either by considering dispersive hydrogen diffusion or local atomic relaxation involving the breaking of an stressed Si-Si bond [7]. The hydrogen content (4%) in our nc-Si:H samples grown at low substrate temperatures is expected to be significantly higher than that in high temperature (>450 ºC) samples used by other groups [5]. However, the enhanced stability of our low temperature TFTs seems to indicate that hydrogen diffusion is not the main factor causing degradation. These results agree with those reported by other groups [7] who did not find any correlation between stability and hydrogen content. By contrast, they found a strong increase in the threshold voltage shift for samples with high microstructural compressive stress favouring the breaking of weak Si-Si bonds. On the other hand, our low substrate temperature samples showed a very slight microstructural stress, as determined in a previous work by X-ray diffraction [8].

4. Conclusions

Bottom-gate nanocrystalline silicon TFTs were deposited at very low substrate temperatures (150ºC) by Catalytic Chemical Vapour Deposition. These devices showed an enhanced stability upon prolonged gate bias stress times compared to some of their counterparts. This enhanced stability seems not to be related to the hydrogen content but to a lower intrinsic microstructural stress. Nevertheless, further work is necessary to determine and understand the factors causing the degradation of the field-effect mobility and the threshold voltage shift after prolonged gate bias stress.

Acknowledgements

This work has been supported by CICYT-TIC 99-084-C03-01.

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Figure captions

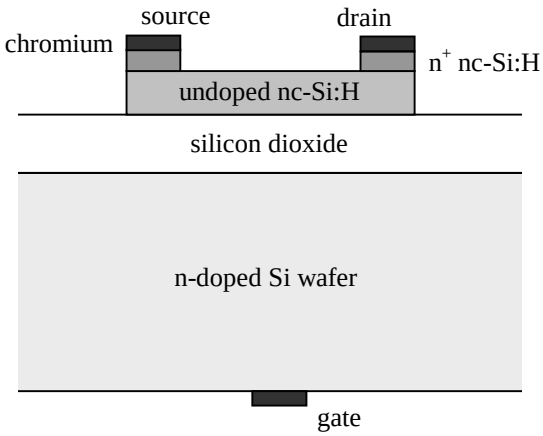
Fig. 1. Structure of the inverted staggered nc-Si:H TFT. Both the undoped nc-Si:H active layer and the n^+-doped one were obtained by Cat-CVD.

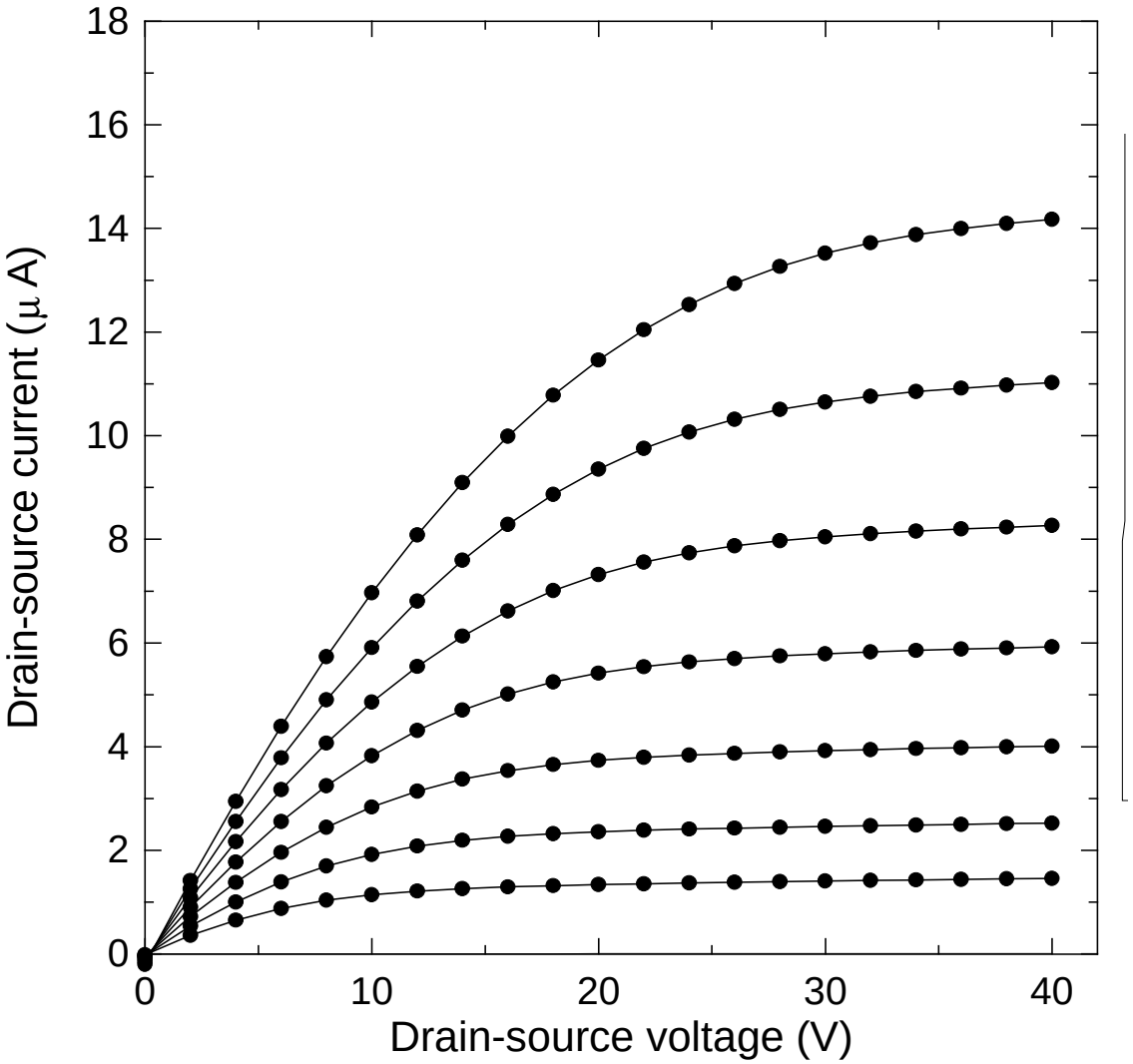
Fig. 2. As deposited output characteristics of the studied nc-Si:H TFTs. Gate-source voltage varied between 12 and 40 V at intervals of 4 V.

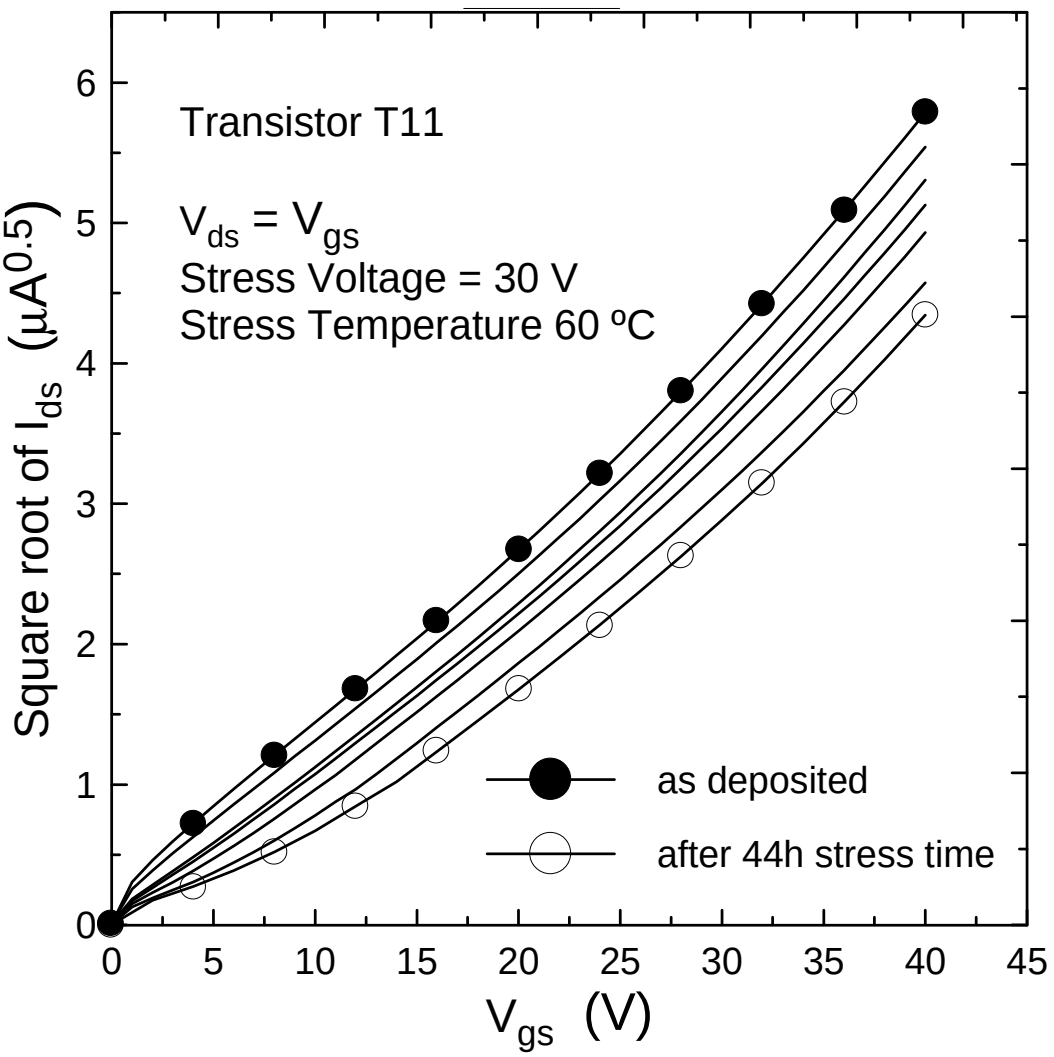
Fig. 3. Saturation characteristics measured during the bias stress degradation experiment.

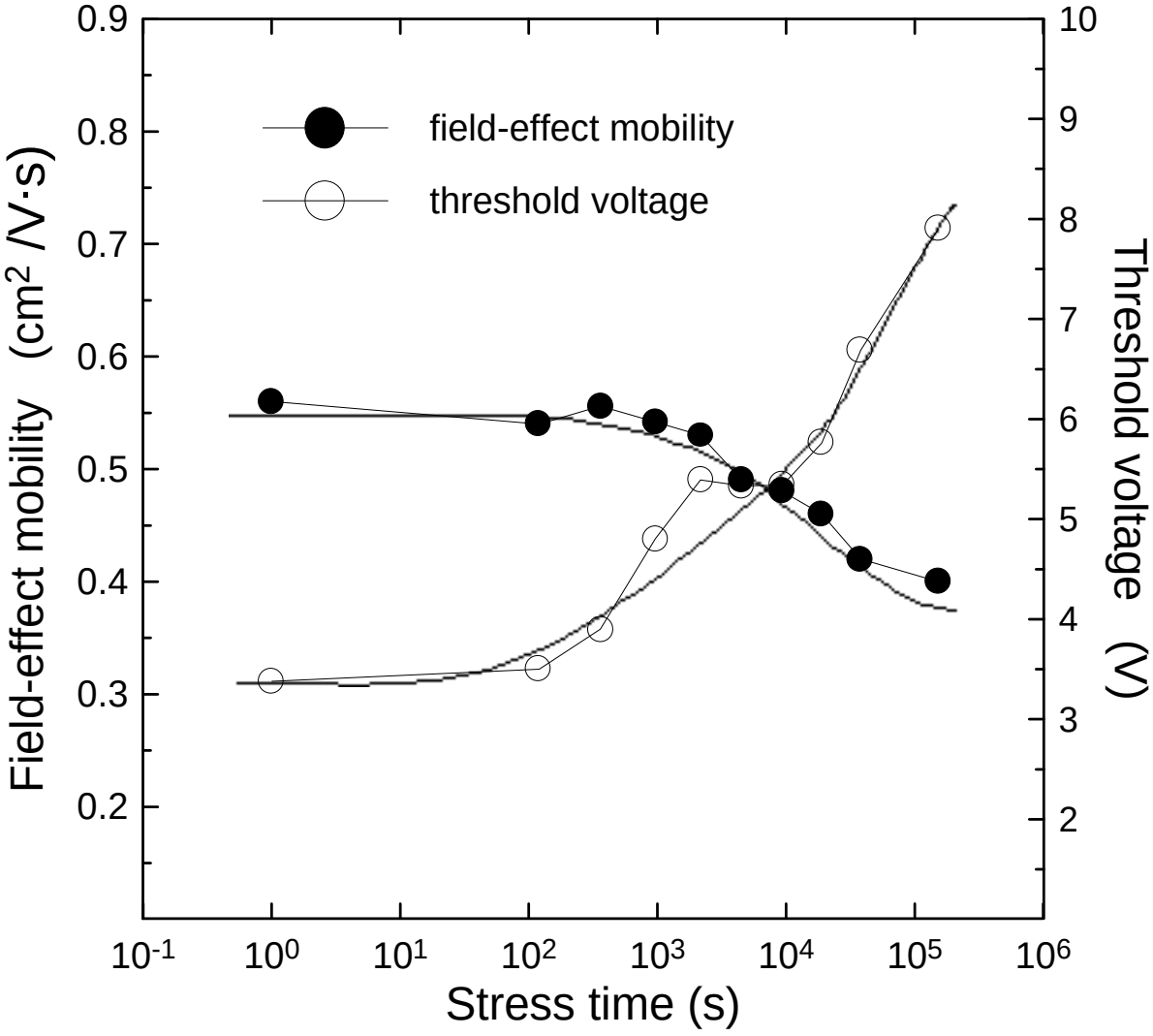
Fig. 4. Field-effect mobility and threshold voltage shift as a function of the stress time.

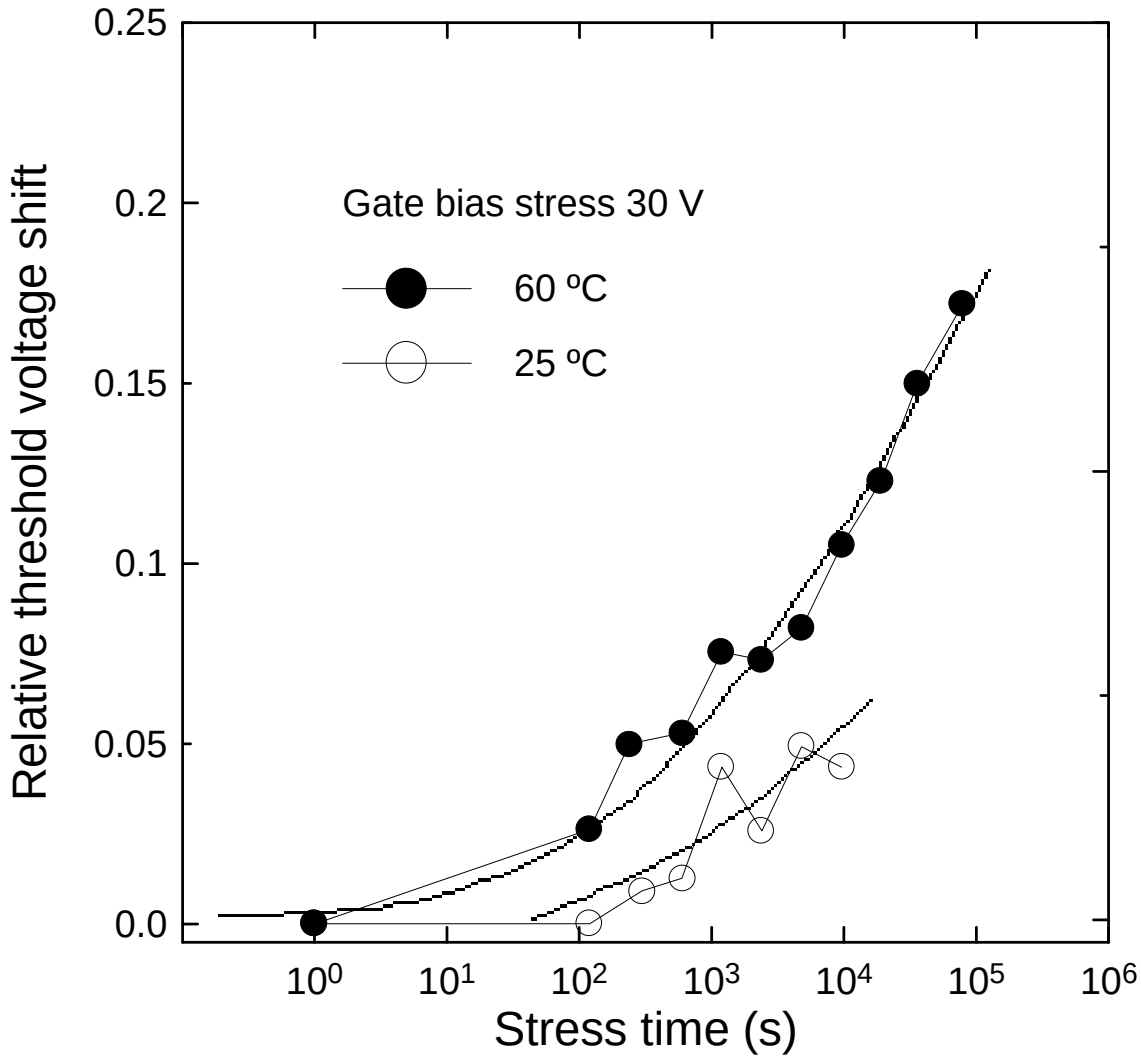
Fig. 5. Relative threshold voltage shift as a function of the stress time for two TFTs degraded at different temperatures.


source
drain
chromium
n+ nc-Si:H
undoped nc-Si:H
silicon dioxide
n-doped Si wafer
gate


Drain-source current (μ A)
Drain-source voltage (V)
0
2
4
6
8
10
12
14
16
18
0
10
20
30
40


Transistor T11
$V_{ds} = V_{gs}$
Stress Voltage = 30 V
Stress Temperature 60 ºC
as deposited
after 44h stress time
Square root of I_{ds} ($\mu A^{0.5}$)
V_{gs} (V)
0
1
2
3
4
5
6
0
5
10
15
20
25
30
35
40
45


field-effect mobility
threshold voltage
Field-effect mobility (cm² /V·s)
Threshold voltage (V)
Stress time (s)
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
10
9
8
7
6
5
4
3
2
10⁻¹
10⁰
10¹
10²
10³
10⁴
10⁵
10⁶


Relative threshold voltage shift
0.25
0.2
0.15
0.1
0.05
0.0
Gate bias stress 30 V
60 ºC
25 ºC
10^0
10^1
10^2
10^3
10^4
10^5
10^6
Stress time (s)