I-IV/P15

Microcrystalline Silicon Thin Film Transistors Obtained by Hot-Wire CVD

J. Puigdollers, *[1] D. Dosev[2], A. Orpella[1], C. Voz[3], D. Peiro[3],
J. Bertomeu[3], L.F. Marsal[2], J. Pallares[2], J. Andreu[3] and R. Alcubilla[1]

[1]Departament d'Enginyeria Electrònica. Universitat Politècnica de Catalunya. Jordi Girona 1-3 Mòdul C4. 08034–Barcelona
[2]Departament d'Enginyeria Electrònica. Universitat Rovira i Virgili.
[3]Departament de Física Aplicada i Òptica. Universitat de Barcelona

Abstract

Polysilicon Thin Film Transistors (TFT) are of great interest in the field of large area microelectronics, especially because of their application as active elements in Flat Panel Displays. Different deposition techniques are in tough competition with the objective to obtain device-quality polysilicon thin films at low temperature. In this paper we present the preliminary results obtained with the fabrication of TFT deposited by Hot Wire Chemical Vapor Deposition (HWCVD). Some results concerned with the structural characterization of the material and electrical performance of the device are presented.

Keywords

1.- Microcrystalline silicon, 2.- Hot-Wire CVD, 3.- Thin Film Transistors.

Introduction

Thin Film Transistors are a prime interest topic because of their application in imagers, printers, and mainly as active elements in large active matrix liquid crystal displays (AMLCD)[1]. These devices are usually obtained using hydrogenated amorphous silicon (a-Si:H) since this material can be easily deposited over large areas at low temperature allowing the use of cheap substrates. However, a-Si:H presents a low mobility and is unstable upon illumination and injection of charge. These aspects cause a-Si:H TFT to be slow devices, sensitive to light and heat. Among the different deposition techniques, Plasma Enhanced Chemical Vapour Deposition (PECVD) is the most used to obtain a-Si:H.

*Corresponding Author:
Tel: +34 934011002, Fax: +34 934016756
E-mail: jpuigd@eel.upc.es

The use of polycrystalline silicon (poly-Si) solves some of the problems previously cited. Polycrystalline silicon does not suffer from metastability and has better mobilities, that translate to display technology with a higher speed, inherent stability, brighter and higher resolution. These advantages are limited by the high processing temperature needed to obtain the poly-Si. For these reasons, there is a lot of research in order to obtain thin film material with properties that combine the advantage of the a-Si:H tecnology (large area deposition and low temperature) with the good electronic properties of polycrystalline silicon (stability and higher mobility). The use of microcrystalline silicon (μc-Si:H) thin film material deposited at low temperature is a good alternative to substitute either for a-Si:H or for polycrystalline silicon. Among the different deposition techniques that are being investigated, the Hot Wire Chemical Vapour Deposition (HWCVD) has drawn a lot of attention because of its capability to obtain device-quality hydrogenated microcrystalline silicon (μc-Si:H) at low temperature over large area [2,3,4]. In the HWCVD technique, gases are dissociated by the catalytic effect in a tungsten filament heated to high temperature (~1700ºC). At first, this technique was basically used to obtain hydrogenated amorphous silicon, and its effectiveness for obtaining silicon thin film material with microcrystalline structure was not showed until recently. In this technique, the substrate temperature, process pressure and the gas composition (silane/hydrogen ratio) determine the structure (ranging from amorphous to microcrystalline) of the film. Recent experimental results reported by different groups confirm the potentiality of the HWCVD technique to obtain intrinsic and doped layers with grain sizes ranging from 0.3 μm to 1 μm at substrate temperatures as low as 200ºC. The good results obtained have encouraged some groups [5,6] to the fabrication of devices (solar cells and thin film transistors).

Experimental

The samples were deposited in a Hot Wire reactor as described elsewhere [7]. The reaction gases, a mixture of SiH_4 and H_2, were dissociated by a tungsten filament (0.5 mm diameter) heated to 1700ºC and the substrates were placed 2 cm above the filament. The substrate temperature was measured by a thermocouple attached to the sample. Deposition parameters were: substrate temperature 280ºC, silane flux 4 sccm and hydrogen flux 76 sccm, and the process pressure was $8\cdot10^{-2}$ mbar. Under these technological parameters the deposition rate was of 2 Å/s. Samples were structurally characterized by Raman Spectroscopy, X-Ray Difraction (XRD) and Transmission Electron Microscopy (TEM).
The TFT used in this work presented an inverted staggered structure which is the most commonly used configuration for flat panel applications. In this structure (figure 1) the gate dielectric is deposited before the μc-Si:H layer. A thermally oxidized n-type (100) silicon wafer with a

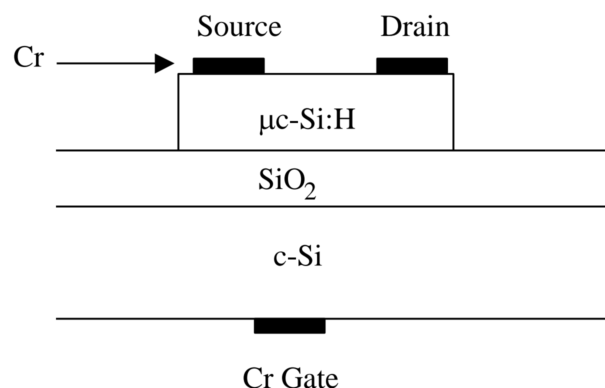

Figure 1. Cross section of the inverted staggered Thin Film Transistor

resistivity of 1-10 Ω·cm was used as a substrate. The thickness of the oxide was 250 nm. The μc–Si:H (250 nm) was deposited at 280 ºC by Hot Wire Chemical Vapour Deposition. Finally, a Chromium layer was thermally evaporated and the metallic contacts (drain and source) were delimited using photolitographic techniques. The channel width (W) was 137 μm and the length (L) 55 μm, giving an aspect ratio for the device (i.e. gate width/length) of 2.5. It is known that the TFT characteristics are dominated by the first nanometers of the layer adjacent to the dielectric interface. For this reason, a pre-treatment of the silicon dioxide surface was done prior to the deposition of the undoped μc-Si:H film. This treatment consisted of exposing the substrate to the influence of atomic hydrogen atmosphere for 15 minutes in the Hot Wire CVD reactor. With this treatment we sought to eliminate surface defects and improve the adhesion of the μc-Si:H film on silicon dioxide. The electrical properties of the TFT were measured under dark conditions at ambient temperature (25ºC) using a semiconductor parameter analyzer (Hewlett Packard 41452B) and a programmable temperature controller (MMR Technologies, inc. K-20).

Results

1. Material properties

In this section we present the structural characteristics of the μc-Si:H film used for the fabrication of the TFT device. Figure 2 displays the Raman spectrum of a μc–Si:H film (0.5 μm) deposited on Corning glass in the same run we deposited the TFT. The sharp peak at 520 cm^{-1} is due to the crystalline phase, whereas the broad peak centered about 480 cm^{-1} is related to the amorphous phase present in the layer. The ratio between the Raman intensities at 520 cm^{-1} and 480 cm^{-1} is usually used as a measure to determine the crystallinity of the film. In our sample the absence of the peak at 480 cm^{-1} together with the presence of a narrow peak at 520 cm^{-1} indicate the crystalline structure of the film. We have also measured the Raman spectrum with the beam incident through the glass, which allows to study the structural characteristics of the films at the first stages of the growth. The results were similar to those on the top surface, confirming the homogeneous structure of the film, and allowing us to ensure the microcrystalline structure of the TFT channel. The TO Raman peak of this layer presented a relative shift of around 3 cm^{-1} and a FWHM of 9 cm^{-1} which corresponds to

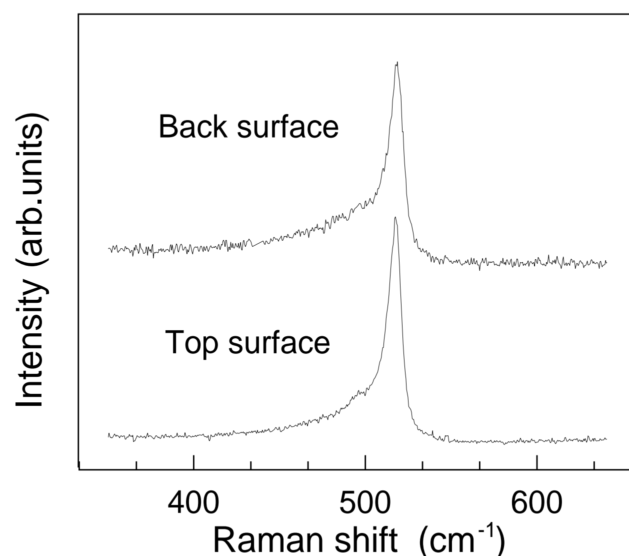

Figure 2. Raman spectrum of the microcrystalline silicon film.

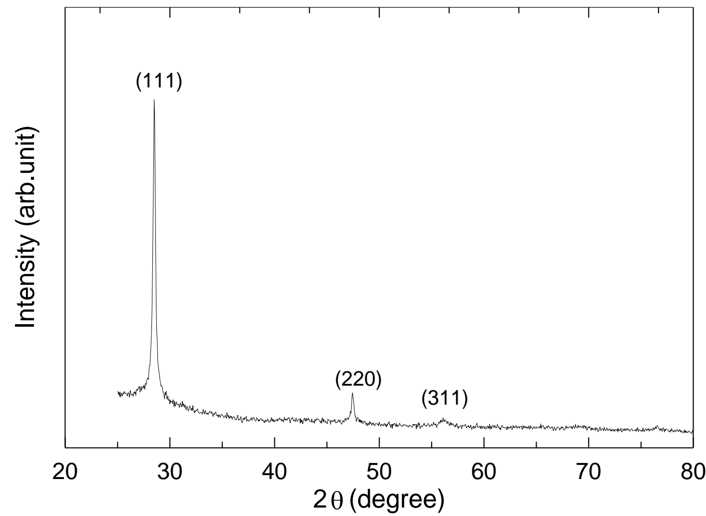

Figure 3. XRD spectrum of the microcrystalline film.

domain sizes of 8 nm by using the confinement model [8]. This fact has also been corroborated by TEM observations.
The crystallinity of the film was also observed by X–Ray diffraction. The θ/2θ plot (figure 3) shows the main crystalline silicon difraction peaks. However the relative intensities of the (111), (220) and (311) peaks do not coincide with those obtained for powder c-Si, which indicate that crystallites are not randomly oriented in the film. The layer has a (111) preferential orientation, although some presence of the (220) is also observed.
The optoelectronic properties of the undoped μc-Si:H layer were: dark conductivity at room temperature: $2\cdot10^{-5}$ $\Omega^{-1}cm^{-1}$; dark conductivity activation energy: 0.5 eV; density of defect states from the Photothermal Deflection Spectroscopy (PDS):< 10^{16} cm^{-3}.

2. Device characteristics

In figure 4 the output characteristics I_{DS} versus V_{DS} at different V_{GS} are shown. The output characteristics show small current crowding (a drain–source current which increases anomolously with increasing V_G, such that the output characteristics for different V_G appear to crowd together) near the origin. This crowding indicates an appreciable influence of the contact resistance of the source and drain electrodes. This effect would be reduced by improving the contact resistance, for example by inserting an n^+ layer between the source/drain and the μc-Si:H layer. Good saturation of the output characteristics for all the gate voltages is also observed. The absence of the kink effect (a rapid rise of the I_{DS} current above a high V_{DS} applied) indicates that the electron injection at the contacts is very small.

In figure 5 the transfer characteristics of the transistor are presented. The application of a gate-source voltage (V_{GS}) leads to an approximately exponential increase of the drain-source current (I_{DS}), followed by a linear increase in current at higher voltages. Drain currents of 1 μA can be obtained for gate voltages lower than 20 V even though the geometry of these devices is not optimized; in particular the aspect ratio is only 2.5. It is known that by increasing the aspect ratio of the device, the on-current and the transconductance would be improved. The relatively high value of the off-current (i.e. for negative gate voltage) is due to the hole current coming from the drain

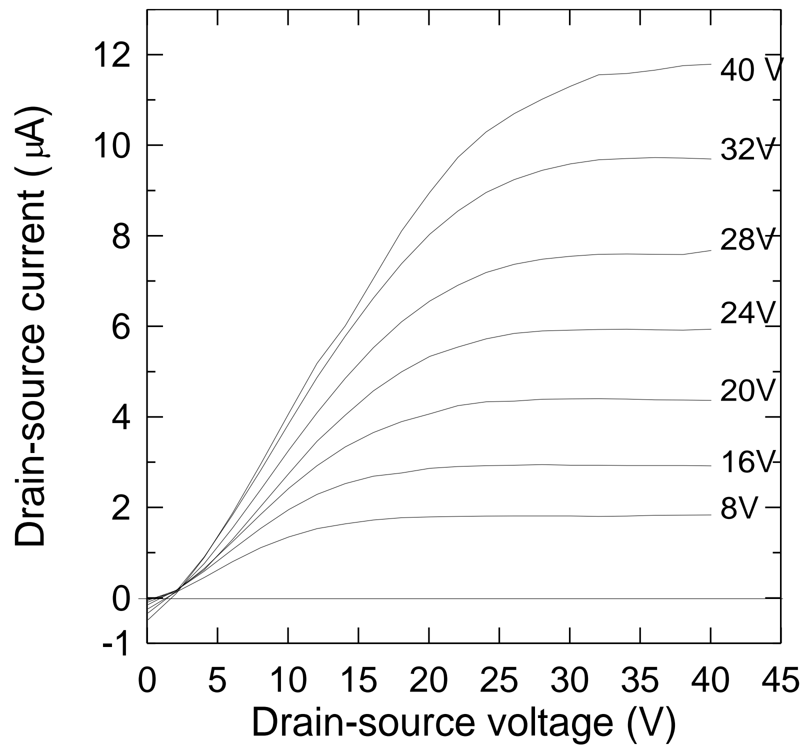

Figure 4. Output characteristics.

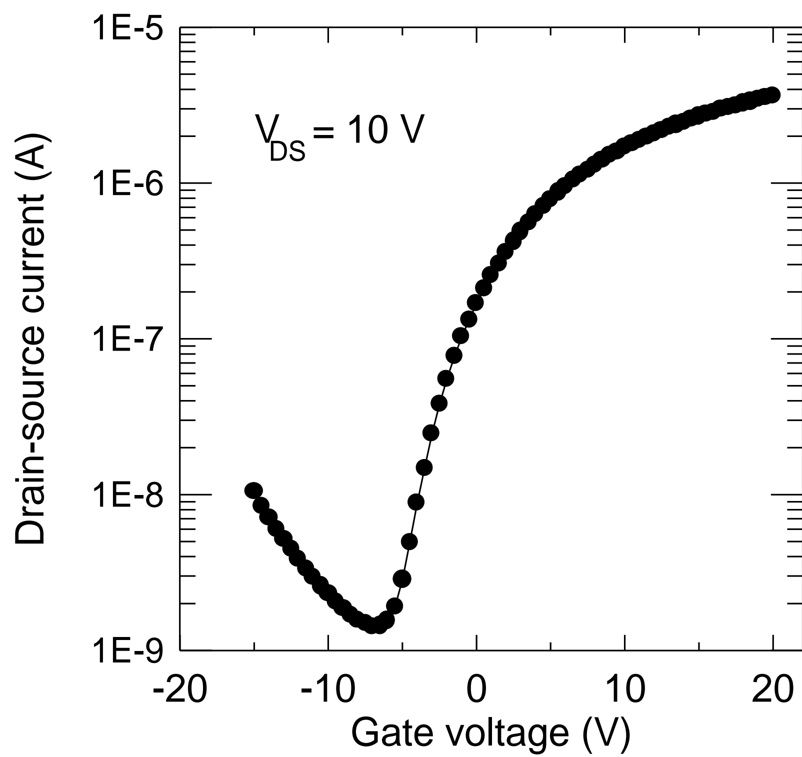

Figure 5. Transfer characteristics of the TFT

and source contacts. This current can be reduced by incorporating a n^+ doped layer between the μc-Si:H layer and the metal contacts. The addition of this n^+ layer not only would reduce the off-current by blocking the hole current, but also would increase the value of on-current by reducing the contact resistance.

The field-effect mobility (μ_s) and the threshold voltage (V_t) can be obtained from the current-voltage characteristics in the saturation regimen, i.e. $V_{GS}=V_{DS}$, where the drain-source current can be approximated by the following expression:

$$I_{DS} = \frac{W}{L}\mu_s C_{ox}\frac{1}{2}(V_{GS} - V_t)^2 \quad (2)$$

where W and L are the gate width and length of the TFT respectively, and C_{ox} is the capacitance of the insulator. By plotting the square root of I_{DS} *vs.* V_G in the saturation regime (see figure 6) we have obtained a mobility value of 0.7 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and a threshold voltage of approximately 0.3 V.

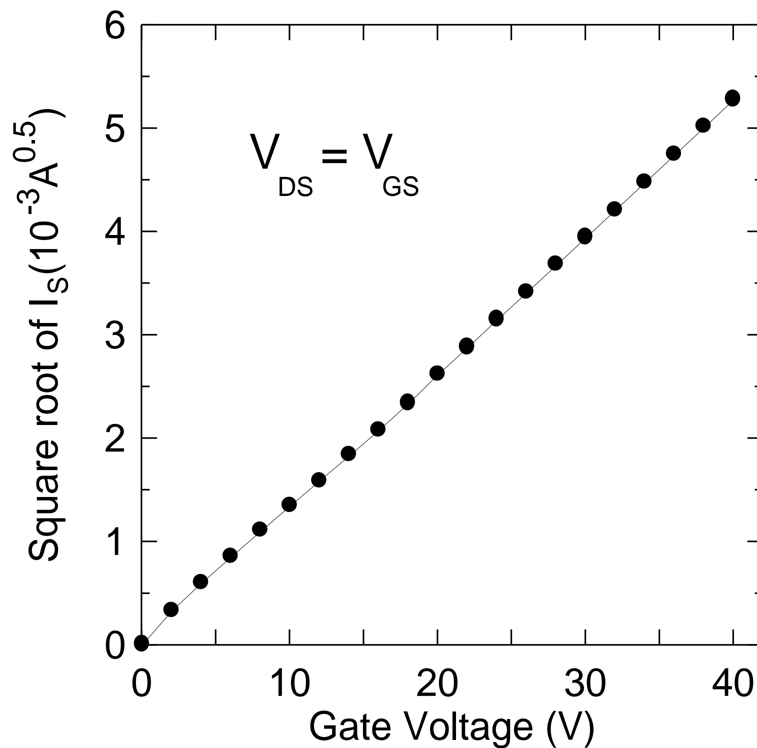

Figure 6. Transfer characteristics of the TFT

These values of mobility and threshold voltage are comparable to those reported in the literature [5], for TFT deposited by HWCVD with similar structure but incorporating an n^+ layer between the drain and source contacts and the μc-Si:H layer .
We have also measured the temperature dependence of the field-effect mobility. Figure 7 shows the mesured μ_s as a function of temperature (from 0 ºC to 80ºC). It is observed that μ_s is thermally activated with an activation energy of 0.1 eV. This value of the activation energy corresponds to an effective charge trap density of about 10^{17} cm^{-3} (see for example Cap. 5 in ref. [9]), in concordance

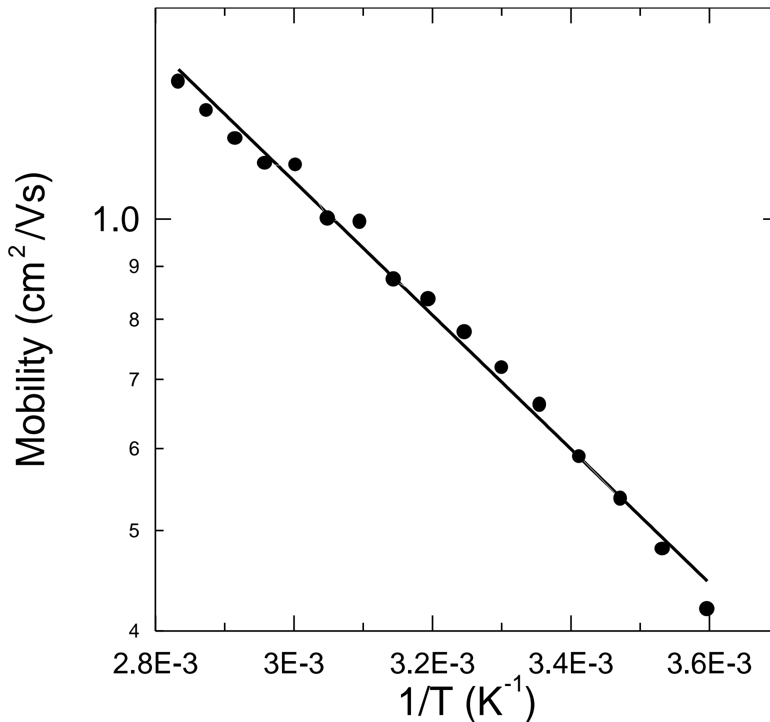

Figure 7. Dependence of the field-effect mobility with the temperature.

with standard Capacitance-Voltage measurements performed on a Schottky structure ZnO/μc-Si:H/Cr [10].

Our future work will focus on two aspects: The first one will be the improvement of the electrical characteristics of the TFTs by incorporating a n^+ doped layer between the electrodes and the μc-Si:H film. The second one will consist of the deposition of the μc-Si:H semiconductor on glass substrates using silicon nitride as a gate dielectric, that should allow us to study TFTs with the same boundary conditions to those of TFTs used as active elements in AMLCD.

Conclusions

In this paper we have presented the preliminary results obtained for TFTs using μc-Si:H deposited at low temperature by Hot Wire CVD. The TFTs had a staggered structure and silicon dioxide was used as a dielectric layer. Microcrystalline thin film material can be obtained by HWCVD at temperatures as low as 280 ºC with good structural and electronic properties. The transistors present satisfactory electrical performance with output characteristics with small crowding effect and good saturation level. A field-effect mobility of 0.7 $cm^2/V\cdot s$ and a threshold voltage of approximately 0.3 V demonstrate the capability of the HWCVD technique to obtain device quality silicon thin film material.

Acknowledgements

The authors would like to aknowledge the contribution of Dr. L. Fonseca from Centre Nacional de Microelectrònica for growing the silicon dioxide. Raman, XRD and TEM measurements were carried out at the Serveis Científico-Tècnics of the Universitat de Barcelona. This work was supported by the CICYT of the Spanish Government under programme TIC96−1058.

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