Phone: +33 (2) 23 23 57 77
Fax: +33 (2) 23 23 56 57
Email: brahim@univ-rennes1.fr

TOP-GATE MICRO-CRYSTALLINE SILICON TFTs PROCESSED AT LOW TEMPERATURE (<200°C)

A. Saboundji[1], N. Coulon[1], A. Gorin[1], H. Lhermite[1], T. Mohammed-Brahim[1], M. Fonrodona[2], J. Bertomeu[2], J. Andreu[2]

[1] GM-IETR UMR-CNRS 6164, Université RENNES I, 35042 Rennes Cedex, FRANCE,
[2] CeRMAE – Dept. Física Aplicada i Òptica, Universitat de Barcelona, 08028 Barcelona, SPAIN

Keywords: Thin Film Transistors, Micro-crystalline, silicon, Low temperature .

Abstract. N type as well P type top gate microcrystalline silicon thin film transistors (TFTs) are fabricated on glass substrates at a maximum temperature of 200°C. The active layer is an undoped µc-Si film, 200 nm thick, deposited by Hot-Wire Chemical Vapor. The drain and source regions are highly phosphorus (N-type TFTs) or boron (P-type TFTs) doped µc-films deposited by HW-CVD. The gate insulator is a silicon dioxide film deposited by RF sputtering. Al-SiO_2- N type c-Si structures using this insulator present low flat-band voltage, -0.2V, and low density of states at the interface D_{it}=6,4 x 10^{10} $eV^{-1}cm^{-2}$. High field effect mobility, 25 $cm^2/V.s$ for electrons and 1.1 $cm^2/V.s$ for holes, is obtained. These values are very high particularly the hole mobility that it was never reached previously.
.

Introduction

Now, the electronic devices, used to process the signal given by mechanical, chemical or biological functions, have to be made on the same substrate used for these other functions. Direct integration of electronics with mechanical, chemical or biological devices increases the reliability, but also, saves place, minimises the power consumption and the maintenance, and decreases the fabrication cost. The most common example is the active matrix flat panel displays that uses field effect thin film transistors (TFTs) made directly on glass substrates. In the Micro-Electro-Mechanical Systems (MEMS) field also, first amplification stage directly at the sensor site is often necessary to improve the signal-to-noise ratio. In many cases, the substrate is a glass or a plastic that does not support high temperature. So, the electronic devices have to be processed at the lowest temperature that can be lower than 200°C in the case of plastics.

The problem deals with the possibility to make electronic devices at low temperature on different substrates with performance with sufficient electrical parameters, depending on the application, but also high reproducibility, uniformity and stability. The basic electronic device is the field effect transistor that includes silicon active layer and source and drain regions as well as high quality gate insulator.

Amorphous silicon based TFTs are currently used in the addressing of the pixels of flat panel displays. The material is deposited at low temperature compatible with the use of plastics. However, the low field effect mobility in these TFTs limits the panel size. Moreover TFTs are subjected to shift of the threshold voltage during the functioning. Finally, the amorphous silicon technology is not able to produce p-type TFTs so that it is not possible to produce CMOS circuits then limiting the practical use of amorphous silicon TFTs in electronics on low temperature substrates.

Then, more stable TFTs with higher electron and hole mobility are needed. Microcrystalline silicon is now the main candidate to reach this goal. It can be deposited by different techniques at low temperature compatible with the use of plastics substrates. It is much more stable than amorphous silicon. Finally it gives hope to reach higher electron mobility and acceptable hole mobility.

Besides the need of device quality silicon, the success in making electronics on low temperature substrates, depends on the possibility to deposit high quality gate insulator at temperature lower than 200°C. This last need is a more hard challenge.

Here, silicon dioxide films are deposited by RF sputtering and then submitted to a plasma post-treatment without heating the substrate holder. Aluminium / RF sputtered SiO_2 / single crystalline silicon wafer MIS structures are used to check the insulator quality of the SiO_2 film.

Microcrystalline silicon films are deposited by Hot-wire CVD.

N type as well P type TFTs, based on these previous microcrystalline silicon and SiO_2 films, are fabricated and characterized.

Experiment

SiO_2 films are first deposited by RF sputtering of SiO_2 target using an Ar/O_2 mixture and without heating the substrate holder, so the temperature reached by the film during deposition is about 80ºC. Capacitance measurements of aluminum / RF sputtered SiO_2 / single crystalline silicon wafer MIS structures are used to optimize the deposition and post-treatment conditions.

Then, N type as well as P type top gate TFTs have been processed using 200 nm-thick microcrystalline silicon (µc-Si:H) film as active layer. The deposition is performed by HWCVD in a multichamber reactor described elsewhere [1]. 2x2 square inch glass covered with 200 nm Atmospheric Pressure CVD (APCVD) deposited SiO_2 are used as substrate.

The configuration of n-type or p-type TFTs is presented in Fig. 1. The process [2] begins by the deposition of a stack of undoped and n-type or p-type doped silicon films. Then, the doped film is plasma etched to form the source and drain regions. The next step is the deposition of 100 nm-thick SiO_2 layer by RF sputtering in the conditions previously optimized. Source and drain contacts are opened through gate insulator and finally aluminum is thermally evaporated and patterned to form the source, drain and gate electrodes. Post-metallization annealing is performed at 200°C in an atmosphere of forming gas. The maximum temperature reached during the process is 200°C that is compatible with the use of many plastics substrates as Kapton E polyimide.

To fix the deposition conditions of the silicon films, we start from the idea that high quality TFTs are induced mainly by the possibility to deposit both undoped and doped films in the same run to improve both the interface and the crystallinity of the up film. Following this idea, the deposition conditions are different for N-type and P-type TFTs.

For N-type TFTs, the undoped film is deposited at a filament temperature T_f ~1610ºC, a total pressure $P = 3 \cdot 10^{-2}$ mbar and a hydrogen dilution of 95% (4 sccm SiH_4 and 76 sccm H_2). The substrate temperature is 200°C. Then the shutter is closed few seconds to avoid the pressure peak due to the introduction of the phosphine and the deposition of the phosphorus *in-situ* doped µc-Si:H layer begins. The ratio [P]/[Si] is 2% in the gas phase.

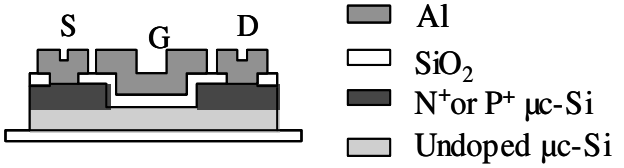

Fig. 1: Cross-section of the *in-situ* doped micro-crystalline silicon (µc-Si) TFT's

For P-type TFTs, we have to take into account that the deposition of highly crystalline and conductive P-type films can be performed only at very low substrate temperature T_S due to the use of diborane as doping gas. T_S is fixed here to 125°C for both the undoped and the doped layers. The undoped film is deposited in the same conditions as previously, only T_S is decreased to 125°C. Then the shutter is closed few seconds to adjust the filament temperature that is increased still 1750°C, to increase the hydrogen dilution (4 sccm SiH_4 and 102 sccm H_2) and to introduce the diborane gas. The ratio [B]/[Si] is 5% in the gas phase

TFTs are then characterized at 300K using a HP4155A semiconductor parameter analyzer. The threshold voltage V_T, the transconductance g_m and the subthreshold slope S are determined from the measured transfer characteristics. V_T is determined in the linear mode by a linear extrapolation on the V_G-axis of the drain current I_D versus gate voltage V_G curve. μ is determined from the maximum slope of this curve that is g_m. S is the minimum reverse slope of the transfer characteristic ($\partial V_{GS}/\partial \log I_{DS}$) measured in the switching region.

Results

Optimization of the SiO_2 deposition and post-treatment. SiO_2 films are deposited by RF sputtering of SiO_2 target using an Ar/O_2 mixture and without heating the substrate holder. Then, the main deposition parameters are : the RF power and the O_2 dilution. To check the effect of these 2 parameters, aluminum / RF sputtered SiO_2 / N-type single crystalline silicon wafer (Al-SiO_2-Si) MIS structures are fabricated. These structures are submitted to a forming-gas annealing at 200°C during 1 hour. The characteristics capacitance-bias (C-V) is measured at high frequency (1MHz), HF-CV, and in the quasi-static regime QS-CV. High quality silicon dioxide can be characterized qualitatively by :

- clear saturation of the quasi-static capacitance
- same insulator capacitance in both the accumulation and the inversion regimes
- HF-CV and QS-CV identical in the depletion and accumulation regimes
- deep minimum of the QS C-V curve
- low flat-band voltage V_{FB}

Taking into account these criteria, both high RF power and O_2 dilution have beneficial effect. However they are not sufficient. H_2+O_2 plasma post-treatment is needed to improve really the C-V characteristics and then the quality of the insulator. Fig. 2 shows the final C-V characteristics at 1MHz and in the quasi-static regime at the end of the optimization. The fifth criteria can be considered as fulfilled.

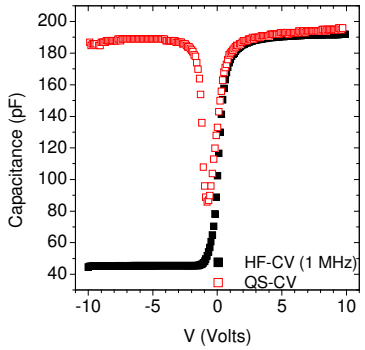

Fig. 2 : Optimized C-V characteristics at 1MHz and in the quasi-static regime. The figure highlights the saturation of the QS curve, the same capacitance in both the accumulation and the inversion regimes, the fit between HF-CV and QS-CV curves in the depletion and accumulation regimes, the

deep minimum of the QS curve and finally the low flat-band voltage V_{FB}. The thickness of the insulator is 67 nm in this case.

The optimized deposition and post-treatment parameters are : 200W RF power, 30% O_2 dilution, and H_2+O_2 plasma post-treatment during 15 minutes. In these conditions the flat-band voltage V_{FB} is -0.2V. The calculated density of states D_{it} at the interface is 6,4 x 10^{10} $eV^{-1}cm^{-2}$.All the C-V characteristics, the low flat-band voltage and the low density of states highlights the very high quality of the present sputtered silicon dioxide fabricated at a temperature maximum of 200°C that is reached during the final annealing. The temperature is fully compatible with the goal to make electronics on plastics substrates.

N-type TFT's characteristics. Fig. 3 and 4 show the transfer and the output characteristics of one typical N-type TFT. The drain current is well modulated by the gate voltage. At fixed gate voltage, it saturates at high drain voltage.

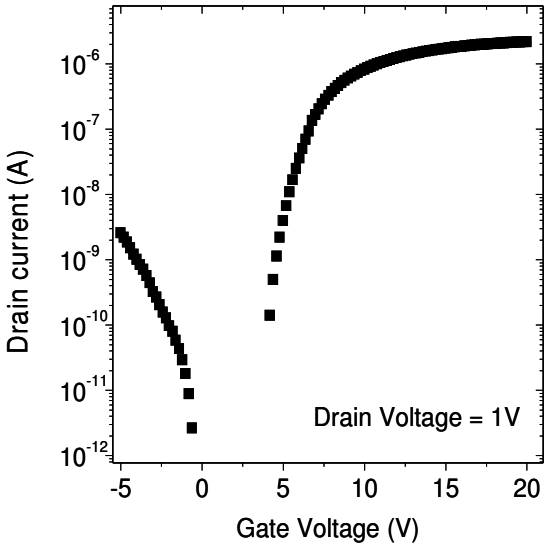

Fig. 3 : Transfer characteristics of N-type TFT measured at a drain voltage of 1V.

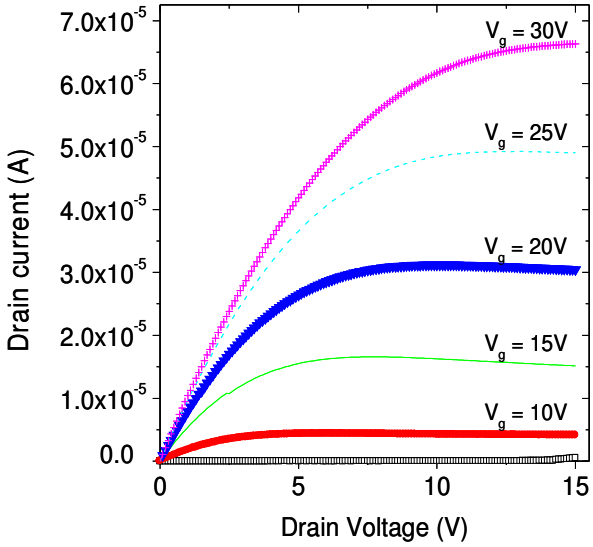

Fig. 4 : Output characteristics of N-type TFT measured at different gate voltage varying from 5V to 30V.

High on to off current ratio is highlighted clearly in Fig. 3. The off current is lower than 1 pA. The output characteristics show the usual saturation of the drain current. The electrical parameters calculated from these characteristics are given in Table 1.

on to off current ratio	Subthreshold slope	Threshold voltage	Electron mobility
> 10^7	0.5 V/dec	6.3 V	25 cm^2/V.s

Table 1 : Electrical parameters of the N-type µc-Si TFTs

The electron mobility is definitively high for µc-Si TFTs. It highlights the quality of the present process that it was improved through the quality of the silicon films, the silicon dioxide, the interface between these two layers, and the technological steps.

P-type TFT's characteristics. Fig. 5 and 6 show the transfer and the output characteristics of one typical P-type TFT. The drain current is well modulated by the gate voltage. At fixed gate voltage, it saturates at high drain voltage

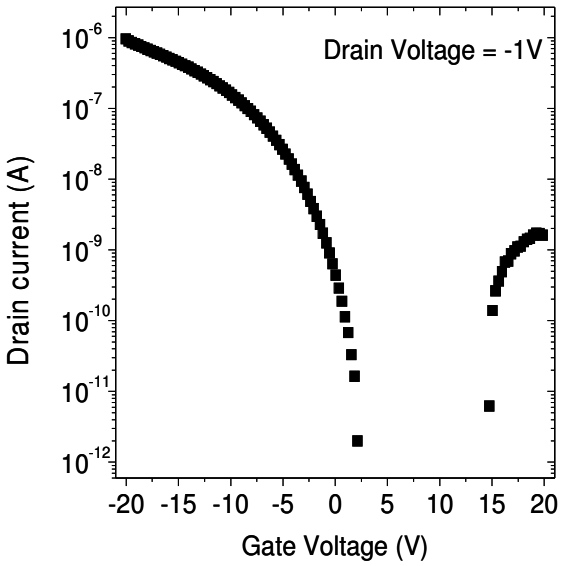

Fig. 5 : Transfer characteristics of N-type TFT measured at a drain voltage of 1V.

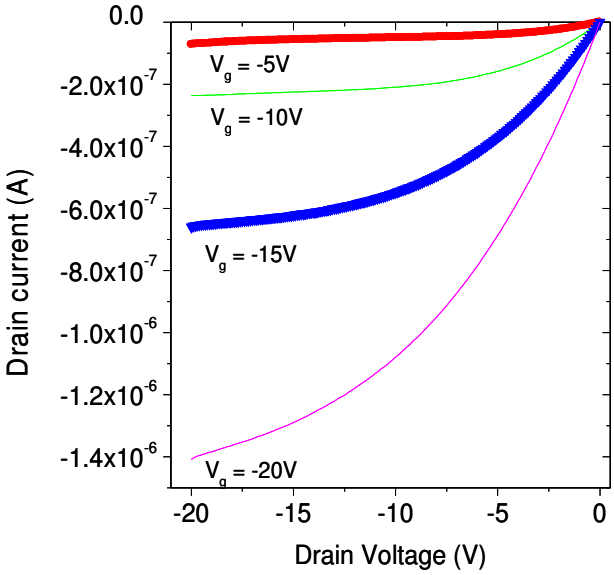

Fig. 6 : Output characteristics of N-type TFT measured at different gate voltage varying from 5V to 30V.

The electrical parameters calculated from these characteristics are given in Table 2.

on to off current ratio	Subthreshold slope	Threshold voltage	Hole mobility
$> 10^7$	0.5 V/dec	-11 V	1.1 $cm^2/V.s$

Table 2 : Electrical parameters of the P-type µc-Si TFTs

All these parameters are really in the high level for p-type µc-Si TFTs. Particularly the subthreshold slope and the mobility were never reached. The present hole mobility is slightly higher than the usual electron mobility of amorphous silicon TFTs. It is high so that CMOS technology based on micro-crystalline silicon deposited at low temperature can be made using the present process in the near future. Previously[3], CMOS inverter using microcrystalline silicon was processed. However, the hole mobility was low (0.031 $cm^2/V.s$) so that the performance of the inverter was poor. Lastly [4], the same group improved the hole mobility still 0.25 $cm^2/V.s$ by using more complicated process.

Conclusion

Full N-type as well as P-type microcrystalline silicon TFT's process was presented. It uses undoped and doped microcrystalline silicon films deposited by HW-CVD at 200°C for N-type TFTs and 125°C for P-type TFTs respectively. The temperature were choosen to be compatible with plastics substrates.

Silicon dioxide acting as gate insulator was deposited by RF sputtering without heating the substrate. The deposition process was optimized through the parameters of Al/sputtered SiO_2/N-type single crystalline structures.

Very high field effect mobility for both N-type and P-type TFTs was obtained. The electron mobility reached 25 cm^2/V.s. The hole mobility was as high as 1.1 cm^2/V.s. Such value of the hole mobility was never reached previously. It gives hope to built a CMOS technology at low temperature based on microcrystalline silicon.

These excellent results are due to the quality of the silicon films, the silicon dioxide, the interface between these two layers, and to the technological steps. Particularly the quality of the interface µc-Si/ sputtered SiO_2 has to be precisely characterized to better understand the previous improvements.

References

[1] C. Voz, D. Peiró, J. Bertomeu, D. Soler, M. Fonrodona, J. Andreu, Mater. Sci. Eng. **B69-70**, 278 (2000)

[2] K. Mourgues, F. Raoult, L. Pichon, T. Mohammed-Brahim, D. Briand and O. Bonnaud, Mat. Res. Soc. Symp. Pro c. **471,** 155 (1997)

[3] Y. Chen, and S Wagner, Appl. Phys. Lett **75**, 1125 (1999)

[4] I.C. Cheng, S. Allen and S Wagner, J. Non-Cryst. Solids **338-340**, 720 (2004)