Residual Thermomechanical Stresses in Thinned-Chip Assemblies

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***Abstract*—A new technology for the three-dimensional (3-D) stacking of very thin chips on a substrate is currently under development within the ultrathin chip stacking (UTCS) Esprit Project 24910. In this work, we present the first-level UTCS structure and the analysis of the thermomechanical stresses produced by the manufacturing process. Chips are thinned up to 10 or 15 μm. We discuss potentially critical points at the edges of the chips, the suppression of delamination problems of the peripheral dielectric matrix and produce a comparative study of several technological choices for the design of metallic interconnect structures. The purpose of these calculations is to give inputs for the definition of design rules for this technology. We have therefore undertaken a programme that analyzes the influence of sundry design parameters and alternative development options. Numerical analyses are based on the finite element method.**

***Index Terms*—BCB, copper, creep, finite element simulation, interconnects, MCM, process modeling, thermomechanical stresses, 3-D integration.**

I. Introduction

ULTRATHIN chip stacking (UTCS) will deliver a new, very dense, three-dimensional (3-D) stacking technology for semiconductor chips. This very dense, ultrathin stacking technology is of interest to all electronics industries where size and weight are important for product acceptance. Another advantage for industry is the possibility of using standard chips from different vendors. The proposed new, dense stack will be based on photosensitive Benzocyclobutene (onwards BCB). The procedure is as follow. The chips are thinned down to 10–15 μm and then, using planarization techniques as used in semiconductor processing, the 3-D stack is formed on a silicon substrate by depositing layers of dielectric, onto which a metallization copper structure is patterned. The thinned chips are placed on top of each dielectric layer and the vertical interconnection is realized with metal vias.

Manuscript received October 6, 1999; revised March 18, 2000. This paper was recommended for publication by Guest Editor B. Courtois upon evaluation of the reviewers' comments. This work was supported by ESPRIT Project UTCS 24910. This work was presented at the Fifth International Workshop on Thermal Investigations of ICs and Microstructures (THERMINIC), Rome, Italy, October 3–6, 1999.

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Publisher Item Identifier S 1521-3331(00)07288-3.

This technology has required the development of a thinning technology applicable to standard finished silicon chips that achieve a final thickness in the order of 10–15 μm using chemical and mechanical procedures [1]. Another challenging point that required some improvements was the development of transport, attachment and bonding solutions for the very thin silicon chips that are used in the 3-D stack. Also the existing planarization techniques used in this stacking methodology had to be duly modified.

During the fabrication process the structure is subjected to a series of temperature excursions, and residual stresses can appear because of the coefficient of thermal expansion (CTE) mismatch between different materials. These process-induced stresses may be high enough to cause early failure of the module.

To be able to study these residual stresses we use a parametric process-modeling framework to simulate the evolution of stresses and strains as the structure is sequentially fabricated. This is in contrast to the usual approach of many researchers who employ a "frozen-view" model starting from the geometry of the final configuration. In the "frozen-view" model, the entire structure is assumed to be stress-free at the curing temperature of the polymer and then cooled down to the room temperature. This procedure provides a better understanding of the process because the material layers are deposited at different temperatures, and therefore, not all layers are stress-free at the same temperature. Furthermore, residual stresses may develop plastic deformations at intermediate process steps, a feature that can not be captured by "frozen models." Previous approaches to solve this problem were based on the addition of artificial nodes or multipoint constraints [2], [3]. However, we base our strategy in the birth/death of elements capability [4], [5]. The details of the implementation of the modeling approach to take into account the entire history of the fabrication process and a general discussion of the features included in our models will be described in Section II.

Thermomechanical simulation of the stresses due to the manufacturing process requires detailed knowledge of the possibly temperature dependent mechanical material properties. Unfortunately they strongly depend on the technological conditions used in the material deposition. Experimental tests have been done accordingly, and from the analysis of the obtained results material models have been optimized. This point is addressed in Section III. In particular we have included stress-relaxation mechanisms for both copper and pre-cured BCB. An additional discussion in this section is raised because of the fact that a thinned chip is far from being a homogeneous slab of silicon. After all the thinning process has reduced the original silicon

substrate to a thickness that is comparable to that of the set of technological layers of metals and dielectrics that conform the active circuitry. That is why we also give an effective material model for this dielectric layer.

As for the results of our calculations many important details of the structure may be captured with a simple two-dimensional (2-D) axisymmetric model. The results of this model are contained in Section IV. With regard to the problems of the interconnection via structures more detailed 3-D models are in order. Several structures have been proposed, and their suitability is discussed in Section V. The final conclusions are summarized in Section VI.

II. Process Simulation

As it has been mentioned in the introduction, we have been confronted with the problem that the geometry of the model cannot be fixed right from the onset. This is because the geometrical position of the elements which form a certain layer, depend on the deformation of the previous layers according to the sequence of technological steps. To simulate the sequential fabrication of the multi-layered UTCS structure, which involves the addition and selective removal of material, we have employed the element birth and death feature in ANSYS 5.4. The entire geometric model is defined from the very beginning, but all the additional layers on top of the substrate are eliminated. From a numerical point of view, this is accomplished by multiplying their stiffness matrices by a reduction factor (10^{-6}). To simulate the sequential deposition of the layers, the temperature loads are applied to the system and the 'dormant' elements are awaked at the effective deposition temperatures.

Moreover, the model includes a number of additional features. Stress relaxation mechanisms in BCB have been included in order to model the BCB behavior at intermediate temperatures prior to complete curing. Copper is modeled as an elastoplastic material with creep. Silicon is modeled as a perfectly elastic material. This procedure permits us to obtain the stresses in the structure along the complete fabrication process, and then it is possible to identify critical points, which may appear at intermediate fabrication steps.

III. Material Models

A. Silicon

Silicon exhibits no plastic deformation or creep below 800 °C. Silicon shows a linear elastic behavior at low strains and transits abruptly to brittle-fracture behavior at a higher strain. While plastic deformation in metals is based on stress-induced dislocation generation in the grain-boundaries and subsequent dislocation migration that results in a macroscopic deformation from intergrain shifts in the material, no grain boundaries exists in single crystal silicon, and plastic deformation can only occur through migration of defects originally present in the lattice or those that are generated at the surface. As the number of this is very low in single crystal silicon, the material is perfect elastic [6].

For the determination of the mechanical properties of BCB and Copper bowing measurements were performed. Wafers were coated with a single copper or BCB layers, and the curvature was recorded as a function of temperature and time. The stresses in the films were calculated from the measurement results using the Stoney equation

$$\sigma = \frac{1}{R}\,\frac{E}{6(1-\nu)}\,\frac{T^2}{t}$$

where

R	measured radius of curvature of the bent substrate;
$\frac{E}{(1-\nu)}$	biaxial modulus of the substrate;
T	thickness of the substrate;
t	thickness of the thin film [7].

The measurement system is based on laser interferometry between the silicon wafer and the extreme of a fiber optic. The wafer is located within a temperature controlled chamber, so the thermal cycling suffered by the thin films during the fabrication process can be replicated. More details can be found in [8].

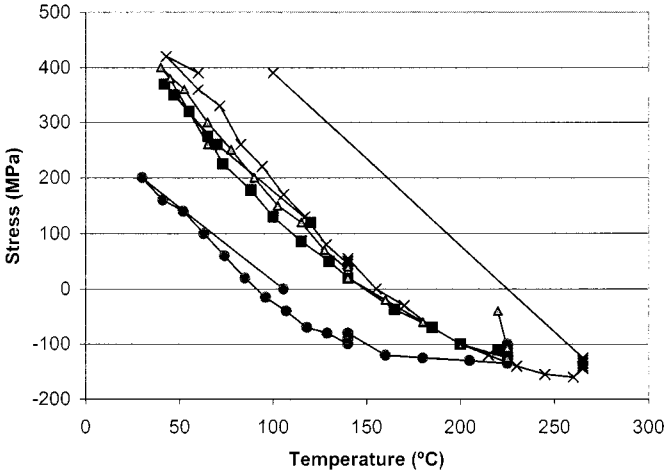

Fig. 1. Thermal stresses against temperature for a 2 μm thick Cu layer on a silicon substrate. The temperature profile imitates the processing steps.

B. Copper

The thermal cycling experiments show indications of relaxation phenomena (Fig. 1). After deposition, the film is in a state of moderate tension. On heating, the tension decreases and the stresses become compressive, with a gradually decreasing slope. On cooling, the stress becomes again tensile up to maxima in the order of 350–400 MPa. Note that these values are much higher than the yield strength of bulk copper, which is reported to be about 100 MPa [9]. On heating again, the stresses describe a hysteresis cycle, which is more evident in the thinner film.

All these behaviors have been previously observed in aluminum and copper films and attributed to different relaxation mechanisms [10]:

1) grain-boundary diffusion;
2) lattice diffusion;
3) low-temperature plasticity;
4) low temperature creep;
5) high temperature creep.

Every relaxation mechanism has a characteristic plastic-strain rate equation. While these effects have been thoroughly studied in bulk copper [11], this is not the case in thin-film copper. In the literature, we can find attempts to qualitatively explain the

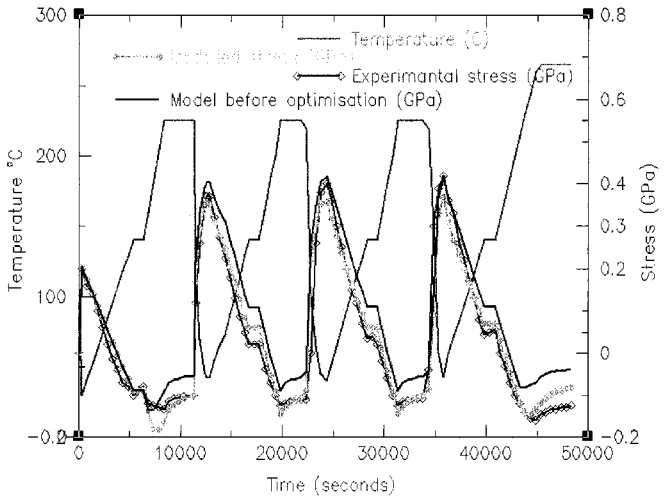

Fig. 2. Comparison of experimental data of thermally generated stresses and copper material models (◇ experimental results, • model results).

shape of the stress curves during thermal cycling [12]. However, a complete agreement between theoretical models and experimental results has not yet been achieved [13].

From the modeling point of view, we can not include five different relaxation mechanisms. Thouless *et al.* [10] have reported on several creep mechanism in the stress/temperature plane. Having in mind the models considered in the literature it may be justified the approximation

$$\dot{\varepsilon} = C\sigma^n e^{-\Theta/T}.$$

where

$\dot{\varepsilon}$ creep strain rate;
σ stress;
T absolute temperature;
C, n, Θ material constants.

Assuming the reported creep parameters for bulk copper, we obtain a qualitatively good agreement between the experimental results and the model predictions. One may obtain a better fit by optimizing the parameters (see Fig. 2). This optimization took the three material constants and tried to minimize the mean square error between the measured stress and the simulated stress in the complete set of temperature cycles. The optimization method uses a mixture of steepest descent and the gradient conjugate method.

For very low temperatures, rate independent plasticity is the more important material nonlinearity. The strain-stress curve has been obtained from Wu *et al.* [4]. A Besseling model (multilinear kinematic hardening) has been assumed for the plasticity model [14].

In Table I a summary of the properties assumed for copper films can be found. Some of them have been extracted from the literature and the creep parameters have been obtained from the optimization work. Although not explicitly given in the table, a temperature dependence for the CTE and Young modulus of copper has been assumed in accordance to the behavior of the bulk material [15].

TABLE I
OPTIMISED COPPER MODEL. THE SYSTEM OF PHYSICAL UNITS MEASURES PRESSURES IN GPa, LENGTHS IN MICRONS, TIME IN SECONDS AND TEMPERATURES IN °K ([15] PLUS OPTIMIZATION IN THIS WORK)

Material Property	**Value**
CTE	16.6 10^{-6} °C^{-1} (300°K)
Poisson ratio	0.36
Young modulus	134 GPa (300°K)
Effective deposition temperature	105.5 °C
Creep parameters (optimised model)	**Value (see caption note)**
C	2200
N	5.7
Θ	5500 °K

TABLE II
OPTIMISED BCB MODEL. THE SYSTEM OF PHYSICAL UNITS MEASURES PRESSURES IN GPa, LENGTHS IN MICRONS, TIME IN SECONDS AND TEMPERATURES IN °K ([16] PLUS OPTIMIZATION IN THIS WORK)

Material Property	**Value**
CTE	5.2 10^{-5} °C^{-1}
Poisson ratio	0.34
Young modulus	2.9 – 0.1 GPa
Effective deposition temperature	120 °C
Creep parameters (optimised model)	**Value (see caption note)**
C1	23.7
N1	2.7
Θ1	2533 °K
C2	11.1
N2	2.1
Θ2	2441 °K

An additional parameter of interest for the FEM modeling is the effective deposition temperature (the temperature at which the elements of the pertinent layer are activated). This temperature has been fitted to reproduce the bowing measurements.

C. BCB

As for BCB we distinguish between two situations: pre-cured BCB and post-cured BCB. For pre-cured BCB we have considered two creep mechanisms, and their parameters have also been fitted by optimization. The material has been modeled in a simple way so as to take into account a progressive softening of the material as the temperature increases. Accordingly its Young modulus at 40 °C is 2.6 GPa and 0.1 GPa at 230 °C (the Young modulus is assumed to vary linearly in-between). A summary of the properties of pre-cured BCB is given in Table II [16]. Fig. 3 shows a comparison with experimental data.

When BCB is cured at 260 °C, it becomes a more stable material. It has been modeled as a perfectly linear elastic model with a Young modulus equal to 4.2 GPa (from nanoindentation measurements [17]) and a Poisson coefficient of 0.34.

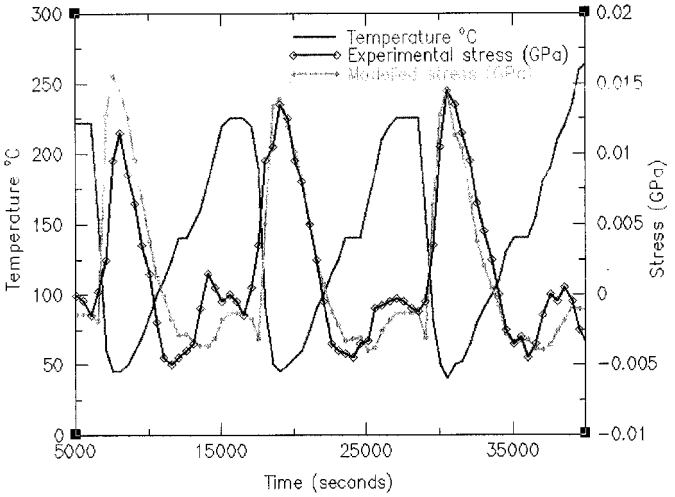

Fig. 3. Comparison of experimental data of thermally generated stresses and an optimized BCB material model (◇ experimental results, • model results).

TABLE III
EFFECTIVE MECHANICAL PROPERTIES OF THE CMOS DIELECTRIC LAYER

CMOS dielectrics-assumed properties	Value
Young Modulus	100 Gpa
Poisson ratio	0.25
CTE	$0.8 \cdot 10^{-6}$ °C^{-1}
Residual stress (nominal)	-75 Mpa
Thickness	3 μm

D. CMOS Dielectric Layer

An additional point of interest is the modeling of the residual stresses induced by the CMOS dielectric and metal layers. While in most packaging models the presence of these layers is neglected in front of the bulk silicon (600 μm thick), it is our belief that this assumption is no longer valid when working with thinned silicon chips. No clear data is available about the residual stresses in these dielectric and metal layers, as far as we know, and these stresses may markedly depend on the technological conditions at issue. Due to that, we have done an explorative study assuming a thinned chip formed by two materials: a thin silicon substrate plus 3 m of a single dielectric layer. CMOS dielectric layers are mainly silicon oxides and oxynitrides. Tentative mechanical properties for this equivalent dielectric layer are summarized in Table III. The mechanical properties are mainly those of silicon oxide, although a higher stiffness has been used accounting for the presence of the oxynitride. A range of compressive biaxial stresses is explored around a nominal value of −75 MPa (from −50 MPa to −100 MPa). All these values have been inspired by the measurements performed on the ES2 technology within the DEMAC Esprit Project 8576.

IV. 2-D AXISYMMETRIC MODEL

A one-layer axisymmetrical UTCS model is represented in Fig. 4. It comprises the thick silicon substrate, a BCB adhesive layer between the thinned chip and the substrate, a copper line and a copper ring. The purpose of this copper ring is to reduce the risk of delamination at the BCB edge.

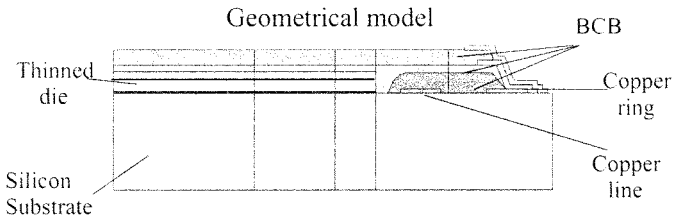

Fig. 4. One-level UTCS 2-D model.

TABLE IV
GEOMETRIC PARAMETERS OF THE 2-D AXISYMMETRIC MODEL

Dimension	Nominal value (μm)	Range (μm)
1) BCB	3	2-4
adhesive	10	8-15
2) Thin chip thickness	2	-
3) Copper line thickness	20	-
4) Copper line width		

A nominal geometry has been analyzed, whose critical dimensions are in Table IV. Deviations from this nominal geometry have been analyzed to study the structure behavior in front of dimensional changes. These studies have to be the input information for design rule definition.

An additional value, whose influence has been considered, is the residual stress in the CMOS dielectrics. Compressive stresses between 50 and 100 MPa have been assumed.

A. Nominal Geometry Results

To our understanding the model presents three areas which can be a source of problems.

1) Thin-chip edge: stresses induced by different TCE.
2) Copper line: stresses induced by different TCE.
3) Copper ring: reduction of stresses in the BCB caused by the copper ring, which is then mechanically loaded by the BCB deformation

In every case, the stress and strain distribution has been obtained and inspected for critical values.

A major source of problems could be BCB, which is the most compliant material in the structure. BCB failures can be cohesive or adhesive. Of course, reliability is established by the weakest link. Experiments performed by Dow Chemical [18]. show that the nature of delamination in BCB/silicon structures was cohesive in the BCB. Typical maximum elongation and tensile strength of BCB is available from the literature. However, due to film variability, problems may appear at values below these limits. Equivalent stresses about 70 MPa can be of concern.

B. Thin Chip Corner

Tensile normal stresses about 80 MPa can be observed in the silicon part of the thinned chips near the edge (see Fig. 5). These

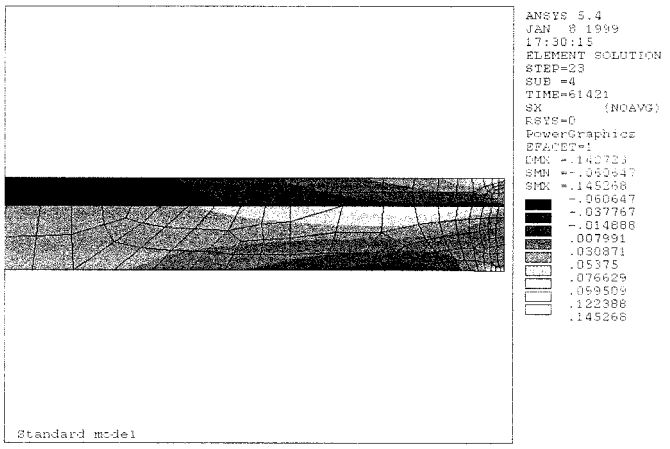

Fig. 5. Stress tensile state of the silicon part of the thinned chip (GPa).

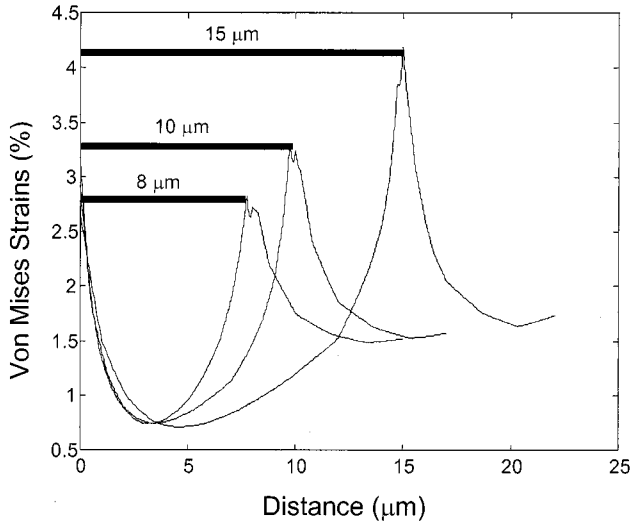

Fig. 6. Von Mises strains (in %) in the BCB matrix along the chip side wall for dfferent chip thicknesses. The straight lines indicate the stretch of the path adjoining the thinned chip in every case.

stresses are the reaction to the compressive state of the dielectric CMOS layer. Anyway these stresses vanish rapidly toward the interior or the chip where the active electronics is located, and 80 MPa do not endanger the reliability of silicon as these values are routinely encountered in silicon pressure sensors. A critical point for BCB is the upper thin-chip corner where Von-Misses strains up to 4% may arise (see Fig. 6). However these strains are very local to the chip corner and they will depend drastically on the corner geometry and mesh. While these levels remain within safe limits in the studied range (from 8 to 15 μm thick chips were considered), an extrapolation of the observed behavior will predict the onset of problems for chips thickness about 40 μm. Nevertheless this value is much bigger than those considered in the UTCS project.

1) Copper lines: Copper lines appear in tensile (roughly biaxial) state with maximum normal stresses about 360 MPa as expected from the thermal cycling experiments.

2) Copper ring: The copper structure is loaded in flexion by the BCB (see Fig. 7). This load introduces a stress concentration at the base of the overhanging copper. This might be of concern

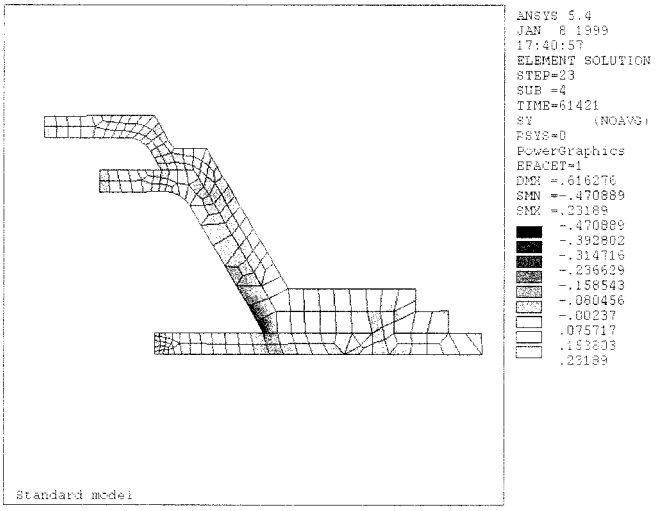

Fig. 7. Normal stresses (σ_{yy}) in the outer copper ring (GPa). For interpretation please refer to Fig. 4.

as a possible fatigue issue, but it may also depend upon the precise geometrical description of the model.

An important conclusion of this preliminary study is that these three critical regions are independent from each other. So changes in the geometry in a critical region will not induce any change in the other regions. This is because in-wafer-plane dimensions are much bigger than vertical dimensions. This fact also explains the negligible effect of the chip side dimension and chip-to-border dimension on the local stress distributions, as we will remark again later on.

All the analysis up to now refer to the strain and stress distribution at room temperature after the fabrication process. However, it is clear that the stresses within the structure must become more severe as the temperature decreases. We have considered a minimum storage temperature of $-55\,^{\circ}$C. At this temperature all the structure suffers from a larger thermal load and consequently all the stresses increase. As expected the copper outer ring may suffer considerable compressive stresses. An important increase is also observed in the BCB at the upper chip corner, with values approaching 6%.

A thorough parametric study was performed varying a wide range of geometric and mechanical variables. These studies reveal that many parameters are quite irrelevant as far as thermomechanical stresses are concerned: chip-to-border distance (1000 to 5000 μm), top BCB thickness (1 to 3 μm), and adhesive BCB thickness (2 to 4 μm). We also considered different chips sizes (from 5 to 25 mm), and no mechanical effects could be attributed to this parameter. If some effect is empirically observed it should be attributed to technological problems regarding BCB spreading or perhaps chips attachment to the adhesive.

V. Three-Dimensional Via Structures

For the realization of electric contacts within the dielectric matrix it was necessary to devise new via structures to go over the slopes between different metal levels. These high aspect ratio via(HARVI) structures are made with electroplated copper. An image thereof may be seen in Figs. 8–10. In fact three different models were proposed. In all of them the via connects a

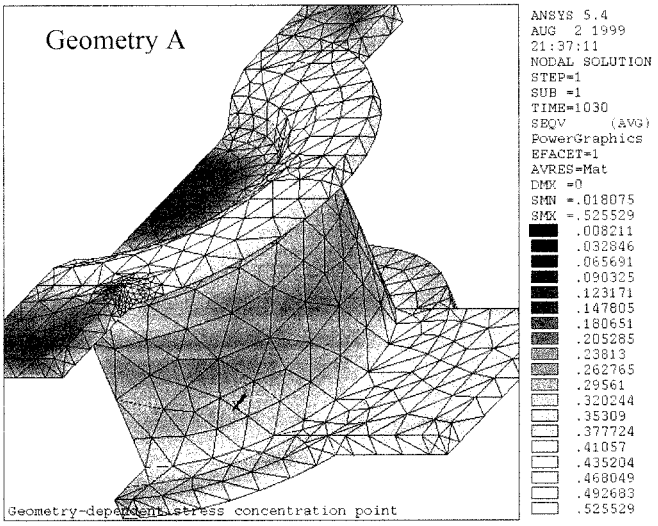

Fig. 8. Upper line descends to meet the stud (GPa).

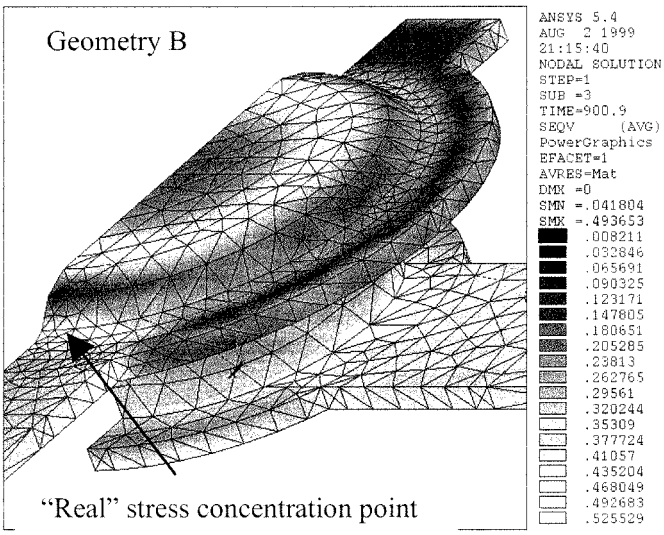

Fig. 9. Upper line ascends to meet the stud (GPa).

20 μm wide and 2 μm thick copper line on the silicon substrate with a second copper line with the same dimensions which starts from the via and runs orthogonal to the first one. This second copper line is on top of a 15 μm thick BCB:

Geometry A: Both lines are connected through an electroplated copper stud. However, the upper line has to descend to meet the stud (Fig. 7).

Geometry B: Differs from geometry A because the upper copper line runs lower than the copper stud and has to climb to meet the stud (Fig. 8).

Geometry C: This model would be an attempt to carry over a standard sputtered nonfilled via into the UTCS technology. In particular no electroplated copper stud is used. The upper line descends 10 μm to find the bottom line (Fig. 9).

In the absence of more information, the mechanical properties of electroplated copper have been assumed to be the same as those for sputtered copper (with the exception the effective deposition temperature, which has been assumed to equal 20 °C).

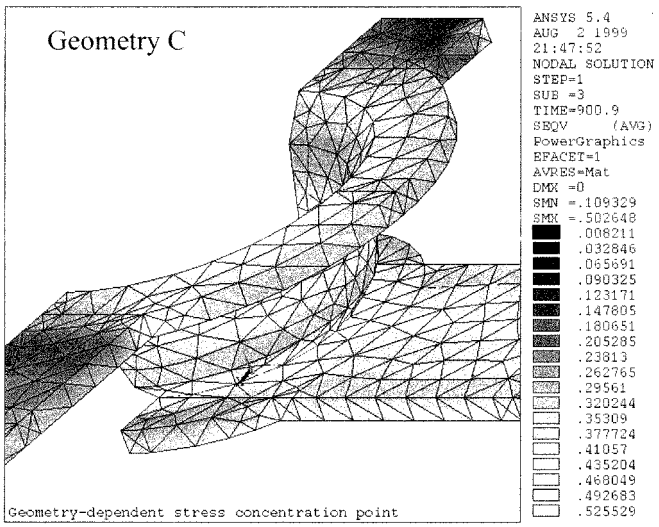

Fig. 10. Traditional nonfilled via: Von Mises stresses (GPa).

The von Mises stresses appear in the Figs. above for these models. Several interesting conclusions can be drawn. High equivalent stresses approaching 500 MPa appear in all the models within the via region (but some stress concentration points may be attributed to spurious geometrical features). The surrounding BCB is not strongly perturbed by the presence of the via. Copper studs in models A, B are substantially free of stresses. In model A, the stress in the upper copper line descending toward the stud is about 330 MPa. In model C, very high stresses appear at the lower part of the upper copper line with values approaching 430 MPa. At the base, some local points show stresses up to 500 MPa. Model B also presents high stress levels: the upper Cu line is pulled and the effect of this motion appears at the region where this line reaches the hat-like structure on top of the stud. Stress levels about 470 MPa are calculated. This stress concentration point, in contrast with others commented along this work, has a real existence, and cannot be attributed to a singularity of the geometrical description. Observe that in model A the upper copper line has a BCB *cushion* sandwiched between it and the copper stud, which prevents such stresses from appearing. A comparison of these results indicates that model A is mechanically superior to models B and C.

VI. Conclusion

We have analyzed the problems associated with the evaluation of thermomechanical stresses in a one-level UTCS structure using the finite element method. In order to obtain reliable answers it has been required to design sensible material models, which is one important achievements of this work. A second important point is that according to our results the UTCS technology admits a great freedom with respect to the choice of many design parameters, which leaves open the possibility for it being applied in a wide range of applications. Thirdly we have been able to give a computationally based justification to support the choice of a particular via stud model with respect to other potential alternatives.

ACKNOWLEDGMENT

The authors would like to thank Dr. J. R. Morante.

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Augustín Coello-Vera, photograph and biography not available at the time of publication.