Force-Balance Interface Circuit Based on Floating MOSFET Capacitors for Micro-Machined Capacitive Accelerometers

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***Abstract*—The feasibility of a force-balance interface based on a second-order delta–sigma ($\Delta\Sigma$) modulator for capacitive sensors has been analyzed in order to delimit the requirements to assure system stability for a given set of constraints related to the sensor-modulator system. A $\Delta\Sigma$ modulator based on a switched-capacitor architecture with floating MOSFET capacitors has been implemented using a 0.7-μm CMOS process. Nonlinear effects related to voltage dependence of the floating MOSFET capacitors have been avoided using a modulator architecture based on charge integrators. The behavior of the new proposed modulator has been measured experimentally and compared with an equivalent interface made with lineal capacitors. Similar results were obtained from both systems. In both circuits, the modulator resolution was better than 14 bits at a sample frequency of 250 kHz, and oversampling ratio of 256.**

***Index Terms*—Accelerometers, delta–sigma ($\Delta\Sigma$) modulators, force-balance (FB) interfaces, MOSFET capacitors, switched-capacitor (SC) circuits.**

I. Introduction

HIGH-performance accelerometers are increasingly needed in automobile air-bag systems, navigation, seismometry, and space applications. Many transduction techniques and several devices with tens of micro-g resolution have been reported [1], [2]. Considerations such as cost, yield, performance, and power consumption [3] are powerful incentives for integrating these devices together with analog and mixed-signal circuits, such as data conversion, on the same chip [4] or in two-chip implementations [5].

Oversampling techniques based on $\Delta\Sigma$ modulation have been widely applied to implement the interfaces between analog and digital signals in VLSI systems [6]. This approach is relatively insensitive to imperfections in circuit components and offers numerous advantages for the realization of high-resolution analog-to-digital converters (ADCs) in comparison with Nyquist-rate converters. There are a number of architectures that can be used for the modulator, but probably, the most robust way of implementing a delta–sigma ($\Delta\Sigma$) converter is by using switched-capacitor (SC) techniques. A signal-to-noise distortion ratio (SNDR) of 94 dB over 250-kHz bandwidth has been reported for a monolithic $\Delta\Sigma$ modulator implemented using SC circuits [7].

The objective of this work has been to demonstrate the possibility of implementation of a second-order $\Delta\Sigma$ modulator that can deliver an adequate dynamic range suitable for its application in capacitive sensor interfaces, using low-cost CMOS technology, and, try to solve two of the main drawbacks that arise from this task: ensure system stability for closed-loop operation, and optimize the large additional area used for the various capacitors in the SC interface.

The paper is organized as follows, after the introduction presented in Section II, we provide background on the capacitive accelerometer model and characteristics, and present the most popular measurement techniques for micro-machined capacitive sensors. Afterwards, in Section III, some aspects related with the design of a force-balance (FB) interface design are discussed, with special emphasis on the analysis of system stability. In Section IV, we present a $\Delta\Sigma$ modulator SC architecture based on floating MOSFET capacitors. Experimental results are presented in Section V, the proposal has been validated by comparing the characteristics of the proposed interface with an equivalent circuit made with lineal capacitors. Finally, conclusions are presented in Section VI.

II. Capacitive Accelerometer Characteristics

In recent years, there is a wide proliferation of capacitive-type sensors in accelerometer applications [8]. The reasons are that capacitive sensors are intrinsically insensitive to temperature, present high sensitivity and resolution, low power consumption and low drift.

A. Accelerometer Capacitive Model

Fig. 1(a) shows the plan view of an accelerometer based on an inertial mass. The inertial mass is used as a reference electrode (E_2), which is between the other two (E_1 and E_3), with the whole system acting as a differential capacitor. When acceleration is applied to the sensor, the mass is displaced, and the distance between the electrodes is modified [Fig. 1(b)]. The capacitance between the terminals E_1 and E_2 (C_{12}), and terminals E_2 and E_3 (C_{23}) can be expressed as

$$C_{12}(x) = \frac{\varepsilon A}{d-x}$$
$$C_{23}(x) = \frac{\varepsilon A}{d+x} \quad (1)$$

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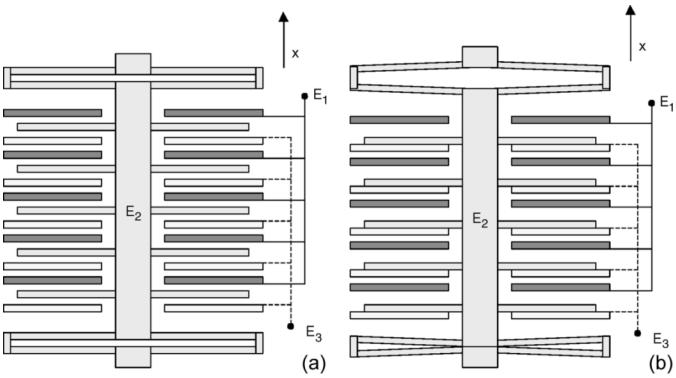

Fig. 1. Accelerometer diagram: (a) in steady state, and (b) under an acceleration in the x-axis direction.

where (ε) is the dielectric permittivity (air in this case), d is the sensing gap distance, A the electrode area, and x is the displacement produced by the acceleration. Measurement of the difference between the capacitors (ΔC) makes it possible to obtain the displacement value

$$\Delta C(x) = C_{12} - C_{23} = 2\frac{\varepsilon A}{d^2\left(1-\frac{x^2}{d^2}\right)}x \cong 2\frac{\varepsilon A}{d}\frac{x}{d}. \quad (2)$$

The displacement is linearly related to the acceleration (α) through the seismic mass (m) and the accelerometer spring constant (K)

$$x = \frac{m\alpha}{K}. \quad (3)$$

Hence, we can relate α with a difference between capacitances as

$$\Delta C(\alpha) \cong 2\frac{\varepsilon A m\alpha}{Kd^2}. \quad (4)$$

By detecting the capacitance changes, we can measure the acceleration. This approximation is valid for small displacements $(x \ll d)$. The dynamic characteristic of the sensor can be modeled by [9]

$$M(s) = \frac{x(s)}{\alpha(s)} = \frac{1}{\frac{1}{\omega_0^2}s^2 + 2\frac{\xi}{\omega_0}s + 1} \quad (5)$$

where ω_0 is the accelerometer resonant frequency, $\omega_0 = \sqrt{K/m}$, $m$the accelerometer seismic mass, and ξ the damping factor. Notice the second-order characteristic of (5).

B. Capacitance Transduction

With recent micromachining technology, this type of sensor can be fabricated with a reduced size. However, the necessary detection of small variation of the capacitance is challenging. Typical sensor capacitance is 100 fF, its variation is only ≈0.1 fF, and it may have to be detected with a resolution of the order of 1 aF [5].

There are three basic measurement techniques for differential capacitive sensors that can be implemented using SC architectures [10]. These are:

- charge amplification (CA);
- charge balance (CB);
- FB.

In CA, a reference voltage $(V_{\rm ref})$ is applied to both capacitors (C_{12} and C_{23}). This voltage introduces an electric charge whose difference is converted into a voltage, using a reference capacitor $(C_{\rm ref})$. We obtain a voltage output signal proportional to ΔC and $V_{\rm ref}$

$$V = \frac{C_{12} - C_{23}}{C_{\rm ref}}V_{\rm ref}. \quad (6)$$

The main drawback of this technique is that it introduces electrostatic forces. Because these forces are proportional to AV^2/d^2, while the capacitance is proportional to A/d, the CA solution is especially adequate for macroscopic sensors, where the distance between electrodes is relatively high.

The CB method tries to balance the electrostatic forces in both capacitors. This leads to a linear interface in capacitive sensors with parallel electrodes, where according to [11]

$$\frac{C_{12} - C_{23}}{C_{12} + C_{23}} = \frac{x}{d}. \quad (7)$$

If the sensor electrodes are not always parallel (as in rotating sensors), we will find intrinsically nonlinear behaviors. In this case the best solution is the FB method, where the proof mass is attained by enclosing the proof mass in a negative feedback loop. The feedback loop measures deviations of the proof mass from its nominal position produced by the acceleration and applies an electrostatic force to keep the proof mass centered. The accelerometer output is taken as the force needed to maintain the position. By maintaining small deflections, nonlinearities are minimized. Because the output is dependent only on the feedback force, the device is first-order insensitive to variations in the mechanical spring constant and $V \propto \alpha$.

We will focus on the last method because it offers the potential of wide dynamic range [1] and is applicable for any sensor geometry [9], although stability aspects must be taken into account during the interface design.

III. Functional Design

There are two basic alternatives for introducing a differential capacitive sensor inside a $\Delta\Sigma$ modulator. The first one is to adapt the input stage of the $\Delta\Sigma$ modulator, but maintaining the modulator outside the measurement loop. The second possibility is to include the modulator inside the loop and take advantage of intrinsic benefits of feedback [12]. The possible disadvantages of this second solution are the difficulty of implementing differential-mode architectures [13] and assure system stability.

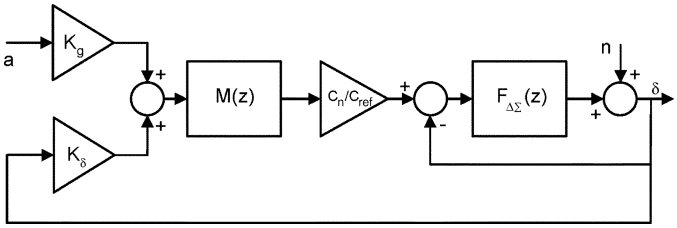

Fig. 2. Transfer function of the sensor-interface system.

A. Modulator Architecture

Choosing the implementation technique and modulator architecture are the first steps of the modulator design process. In this design, the SC technique has been used in the implementation of the proposed modulator. A second-order $\Delta\Sigma$ modulator has been preferred, in order to maximize the ratio between processing efficiency and design effort.

B. Stability Analysis

The accelerometer acts as a second-order filter. The second-order characteristic of (5) with the second-order modulator gives a fourth-order system that can be driven in an unstable condition in a variety of situations (i.e., start up, power-supply bouncing, unbound input signals). In order to design the modulator for a proper functioning, the stable region of operation must be known [14]. The system transfer function can be obtained from inspection of the block diagram presented in Fig. 2

$$H_{\Delta\Sigma}(z) \equiv \frac{\delta}{\alpha} = \frac{K_g \frac{C_\alpha}{C_{\text{ref}}} M(z) F_{\Delta\Sigma}(z)}{1 + K_\delta \frac{C_\alpha}{C_{\text{ref}}} M(z) F_{\Delta\Sigma}(z)} \tag{8}$$

where $C_\alpha = 2\varepsilon_0 A/d$, K_g, and K_δ are the position dependency on the acceleration and the $\Delta\Sigma$ output, $M(z)$ is the accelerometer z-plane transfer function, and $F_{\Delta\Sigma}(z)$ is the $\Delta\Sigma$ modulator one.

$M(z)$ can be obtained from the (5) applying the unity pulse invariance method [15]. The transfer function of a second-order $\Delta\Sigma$ modulator can be written as [7]

$$F_{\Delta\Sigma}(z) = \frac{1}{z^2 + \left(\frac{1}{g_0} - 2P_0\right) z + \left(P_0^2 - \frac{P_0}{g_0} + 1\right)} \tag{9}$$

where (g_0) is the integrator gain, which in SC architectures depends on the capacitors matching. Its ideal value is $1/2$. (P_0) is the fraction of the output voltage that is integrated with the input value. The ideal value is 1, but this is usually lower due to the finite gain of operational amplifiers used to build the integrators

$$P_0 = 1 - \frac{1}{A_V}. \tag{10}$$

The values of C_α, K_δ, ω_0, and ξ can be computed from the accelerometer parameters as [16]

$$\begin{cases} C_\alpha = 2\frac{\varepsilon_0 A}{d} \\ K_\delta = \frac{1}{2}\frac{\varepsilon_0 A}{K d^3} V_{\text{ref}}^2 \frac{1}{1 - 2\frac{\varepsilon_0 A}{K d^3} V_{\text{ref}}^2} \\ \xi = \frac{1}{2}\frac{B}{\sqrt{mK}} \\ \omega_0 = \sqrt{\frac{K}{m}} \end{cases} \tag{11}$$

where B is the accelerometer viscous term and (V_{ref}) a voltage source that generates the electrostatic force. The resulting values for our specific accelerometer are $C_\alpha = 834$ fF, $K_\delta = 0.448$, $\omega_0 = 2.0 \cdot 10^4$ rad/s and $\xi = 1.5$ [11]. The next step is the determination of the z-plane transfer function of the accelerometer applying the unity pulse invariance method to (5)

$$\begin{aligned} M(z) &= K_\delta \frac{B_1 z + B_0}{z^2 + A_1 z + A_0} \\ A_1 &= -2e^{-\frac{a}{f_s}} \cosh\left(\frac{\omega}{f_s}\right) \\ A_0 &= e^{-2\frac{a}{f_s}} \\ B_1 &= 1 - e^{-\frac{a}{f_s}} \cosh\left(\frac{\omega}{f_s}\right) - \frac{a}{\omega} e^{-\frac{a}{f_s}} senh\left(\frac{\omega}{f_s}\right) \\ B_0 &= e^{-2\frac{a}{f_s}} - e^{-\frac{a}{f_s}} \cosh\left(\frac{\omega}{f_s}\right) + \frac{a}{\omega} e^{-\frac{a}{f_s}} senh\left(\frac{\omega}{f_s}\right) \end{aligned} \tag{12}$$

where f_s is the sampling frequency and ω and a, respectively, are

$$\begin{cases} \omega = \omega_0 \sqrt{\xi^2 - 1} \\ a = \xi \omega_0 \end{cases} \tag{13}$$

when $M(z)$ and $F_{\Delta\Sigma}(z)$ are substituted into (8), the result is an expression related to a fourth-order system. Assuming that the acceleration bandwidth is lower than f_s and our accelerometer has a damping factor close to 1, we obtain

$$\begin{aligned} H_{\Delta\Sigma}(z) &\equiv \frac{C_\alpha K_g}{C_{\text{ref}}} \frac{B_1 z + B_0}{z^4 + A_3 z^3 + A_2 z^2 + A_1 z + A_0} \\ A_3 &= \frac{1}{g_0} - 2P_0 - 2e^{-\frac{\omega_0}{f_s}} \\ A_2 &= P_0^2 - \frac{P_0}{g_0} + 1 - 2\left(\frac{1}{g_0} - 2P_0\right) e^{-\frac{\omega_0}{f_s}} + e^{-2\frac{\omega_0}{f_s}} \\ A_1 &= RB_1 - 2\left(P_0^2 - \frac{P_0}{g_0} + 1\right) e^{-\frac{\omega_0}{f_s}} \\ &\quad + \left(\frac{1}{g_0} - 2P\right) e^{-2\frac{\omega_0}{f_s}} \\ A_0 &= RB_0 + \left(P_0^2 - \frac{P_0}{g_0} + 1\right) e^{-2\frac{\omega_0}{f_s}} \\ B_1 &= 1 - e^{-\frac{\omega_0}{f_s}} - \frac{\omega_0}{f_s} e^{-\frac{\omega_0}{f_s}} \\ B_0 &= e^{-2\frac{\omega_0}{f_s}} - e^{-\frac{\omega_0}{f_s}} + \frac{\omega_0}{f_s} e^{-\frac{\omega_0}{f_s}} \end{aligned} \tag{14}$$

where R is a feedback factor defined as

$$R \equiv \frac{C_\alpha K_\delta}{C_{\text{ref}}}. \tag{15}$$

A dependence between ω_0 and the maximum allowed feedback factor can be extracted from (14). To do this, we have substituted z by $e^{i\theta}$, and searched the solutions that have all the poles of the transfer function inside the unity circle. This happens when the feedback factor is lower than a given threshold value labeled as $R_{\max}$ (Fig. 3).

The modulator sampling frequency divided by the oversampling ratio must be greater than the sensor bandwidth. Because

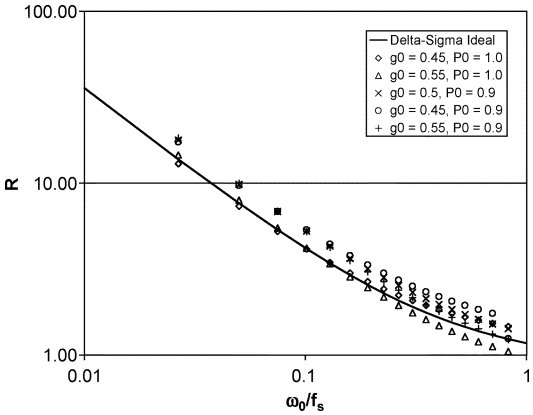

Fig. 3. Feedback factor (R) versus oversampling ω_0/f_s.

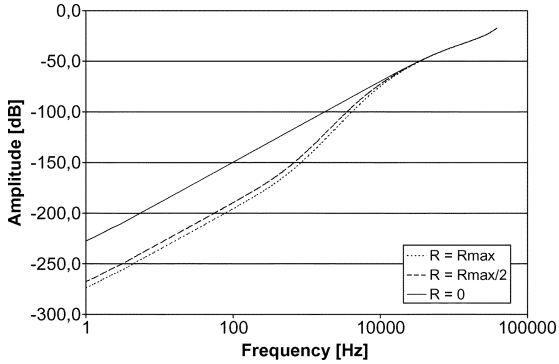

Fig. 4. System resolution versus feedback factor (R).

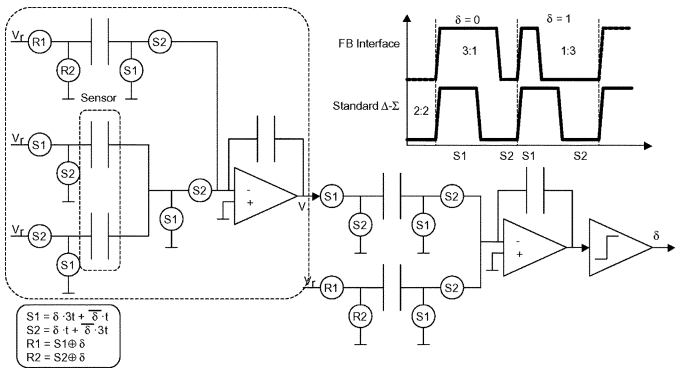

Fig. 5. FB interface schematics. Two phases S1 and S2 with different time amplitude have been generated.

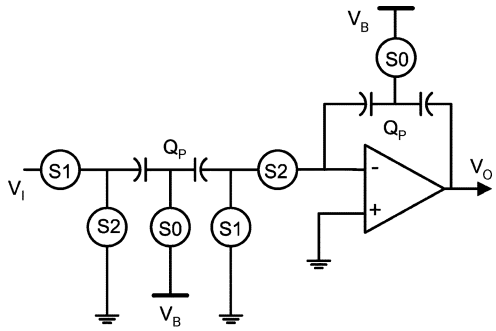

Fig. 6. SC integrator schematics.

$R_{\max}$ and sensor bandwidth are related, is possible to calculate the minimum sampling frequency for a given oversampling ratio.

C. Modulator Parameters

Readout resolution depends on the noise performance of the interface chip, which is mainly determined by front-end charge integrator kT/C noise, input amplifier $1/f$ noise, and switching noise. The dominant thermal noise sources are usually the sampling capacitors of the first stage; thus, the reference capacitor must satisfy

$$C_{\text{ref}} \geq \frac{2kT}{\langle \Delta V^2 \rangle} \tag{16}$$

where k is the Boltzman constant, T is temperature, and (ΔV) the desired voltage resolution. For a modulator resolution of 16 bits working with a reference voltage of $V_r = 2.5$ V ΔV is given by

$$\Delta V = \frac{2V_r}{2^{16}}. \tag{17}$$

Then $C_{\text{ref}} > 1.4$ pF. A feedback factor of 0.23 has been calculated using (15) for a reference capacitor of 1.6 pF. This value is smaller than 1, so it does not affect system stability, as is shown in Fig. 3. and the use of a compensator circuit as described in [17] is not necessary.

The modulator Nyquist frequency is another key parameter. Taking into account the sensor bandwidth, we define it as 2 kHz. This supposes that for a resolution of 16 bits, the sampling frequency must be greater than 1 MHz [7], then $\omega_0/f_s \cong 2^{-3}$, which features a $R_{\max} \approx 100$. Fig. 4 shows the effect of R on the system resolution. Note that the feedback factor related with our accelerometer is very small compared with $R_{\max}$, therefore the system resolution is similar to the one that we have with a second-order modulator.

IV. Circuit Design

The circuit that has been developed is based on a two-phase implementation. This makes possible to measure the difference between the two capacitances of the sensor. The analog part of the modulator is shown in Fig. 5. We also have a digital-to-force modulator based on the different duration of the phases S1 and S2. The output signal (δ) is used to establish this phase duration. When δ is high, the first phase (S1) is three times longer than the second one (S2), while when δ is low, S2 is three times S1. This difference between phase lengths produces an electrostatic force that balances the input force, resulting in the FB implementation. Both synchronizing signals have been generated by an on-chip digital state machine.

The signals $R1$ and $R2$ depend on the output values S1 and S2. They are used to obtain a positive or negative reference charge, depending on δ.

In this context, some features of the blocks are very important and must be optimized. Particular attention was devoted to the design of the operational amplifier, which is the most demanding cell of the architecture. Another key point that requires particular attention is how capacitors are integrated. These devices can occupy a considerable area, and therefore selection of an area-efficient capacitor becomes highly desirable.

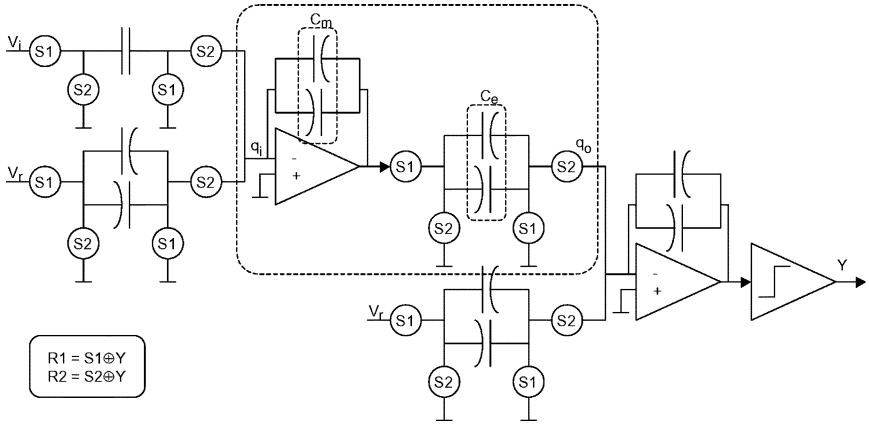

Fig. 7. $\Delta\Sigma$ modulator based on floating-gate capacitors. The charge integrator is shown inside the dashed box.

A. Gate Capacitors

If area has a considerable importance in the total circuit cost function, the native MOSFET capacitors (or gate capacitors), widely available in any digital process, seem to be a promising alternative to avoid the use of more expensive processes. They present higher values than double poly capacitors and good matching properties. Relative mismatching as low as 0.02% has been reported [18]. For this option, it is necessary to assure that it is possible to compensate for or correct their strong voltage dependence in order to minimize their affect on the performance of the modulator [19].

Instead of choosing a single MOSFET gate as a basic capacitive structure, we have used a couple of floating gate capacitors connected in antiparallel. In this structure the capacitance of both gates is enhanced in such a way that dependence on voltage is reduced.

B. Switch Capacitor Circuits Using Gate Capacitors

The use of MOS capacitors inside a SC circuit has been previously considered as an alternative to metal or double poly capacitors, and high-performance $\Delta\Sigma$ implementations based on MOS capacitors have been reported [20]. Most of these reported solutions are based on fixing the operation point of MOS capacitors in their accumulation region, where the capacitor presents its maximum capacitance and minimum voltage dependence. A different approach is proposed in this work. The behavior of the MOS capacitor can be expressed as

$$C(V) = AC_0 f_V(V) \tag{18}$$

where A is the capacitors area, C_0 is a scale factor related to technological parameters and is independent of the voltage between the capacitor terminals (V), and $f_V(V)$ is a nonlinear function that collects all voltage dependences. In linear capacitors C_0 is the capacitance per unit area and $f_V(V) = 1$. Therefore, the charge-voltage relation is given by

$$Q(V) = AC_0 f_V(V)V \tag{19}$$

where Q is the charge stored in the capacitor.

Using the charge conservation law, we obtain the integrator discrete-time equations for the SC integrator (Fig. 6)

$$\begin{cases} Q_i[n] = A_i C_0 f_V\left(V_i[n]\right) V_i[n] \\ Q_o[n] = Q_o[n-1] + Q_i[n-1] \\ V_o[n] = \frac{Q_o[n]}{A_o C_0 f_V(V_o[n])}. \end{cases} \tag{20}$$

Although the charge integration process is linear, the integrator output, $V_o[n]$, is accumulating the nonlinearities of the input capacitor (C_i), introducing harmonic distortion.

A different result will be obtained from the analysis of the charge integrator presented in the schematics of Fig. 7. In this case, we consider that the input and the output signals are charges instead of voltages. The charge integrator is described by the following discrete-time difference equations:

$$\begin{cases} Q_m[n] = Q_m[n-1] + Q_i[n-1] \\ V_m[n] = \frac{Q_m[n]}{A_m C_0 f_V(V_m[n])} \\ Q_o[n] = A_o C_0 f_V\left(V_m[n]\right) V_m[n]. \end{cases} \tag{21}$$

These equations can be rewritten as

$$\begin{cases} Q_o[n] = A_o C_0 f_V\left(V_m[n]\right) \frac{Q_m[n]}{A_m C_0 f_V(V_m[n])} \\ Q_m[n] = Q_m[n-1] + Q_i[n-1] \end{cases}. \tag{22}$$

The expression (22) can be simplified, obtaining a set of difference equations that only depend on area ratios between capacitors

$$\begin{aligned} Q_o[n] &= \frac{A_o}{A_m}\left(Q_m[n-1] + Q_i[n-1]\right) \Rightarrow \\ Q_o[n] &= \frac{A_o}{A_m} Q_i[n-1] + Q_o[n-1]. \end{aligned} \tag{23}$$

The resulting charge integration process is linear assuming that we use gate capacitors that have the same voltage dependence and C_0 (as occurs with the MOS gates inside a VLSI die). In our particular application, the accelerometer gives a charge input $Q_i[n]$; thus we can take advantage of linear properties of charge integrators, and there is no need of linear capacitors if we are able to work with signals related to charges.

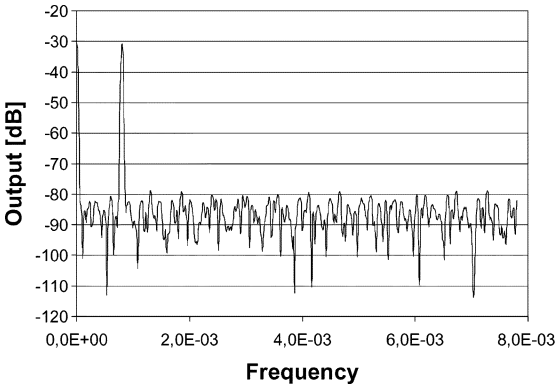

Fig. 8. Measured spectrum ($f_i = 200$ Hz, $f_s = 250$ kHz). The x-axis has been normalized to the sampling frequency. Noise floor is located at -85 dB.

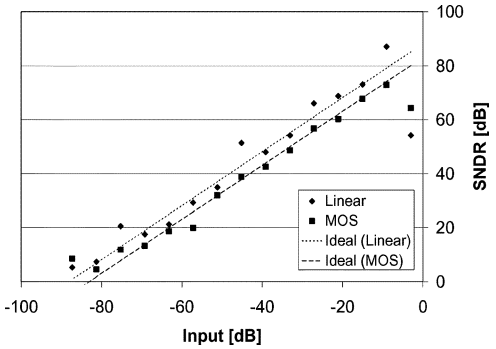

Fig. 9. SNDR with a sampling frequency of 250 kHz and an oversampling ratio of 32. The differences observed between the two modulators can be related with the different ratio between the metal input capacitor and the MOS reference capacitor ($\approx$3 dB).

C. OTA Implementation

The integrators in the modulator have been implemented using gate capacitors and operational transconductance amplifiers with folded-cascode topology [21].

Practical implementations of SC circuits require high gain in order to insure sufficient linearity and parasitic insensitivity in the integrator response. An amplifier gain of 60 dB has proven to be adequate in high-resolution applications [7]. The specifications for the OTA were slew rate of 25 V/μs and gain bandwidth of 10 MHz.

V. Test

The proposed modulator has been integrated in a standard single-poly, double metal 0.7-μm CMOS technology using device-level layout automation tools [22]. We have placed two identical interfaces in the same chip, a MOSFET-only version using floating MOSFET capacitors and a second one using metal capacitors. The active die area (excluding pads) is about 1.7 mm^2. The digital circuits are physically separated from the analog section and are powered from a separate supply. Dummy capacitors, placed along the outside edge of the capacitor array, guarantee that the fringing fields at the periphery of the array are identical to those in the interior. Measurements were performed to determine the behavior of both modulators versus sampling frequency.

Fig. 8 shows the output spectrum of a 65536 samples bit stream. The result plotted in Fig. 9 show the absence of noticeable harmonic distortion in the floating MOSFET interface above the noise floor level.

The SNDR has also been obtained as

$$\mathrm{SNDR} = \frac{P_{\mathrm{Signal}}}{P_{\mathrm{Noise}} + P_{\mathrm{Distortion}}} \tag{24}$$

where P_{Signal}, P_{Noise}, and $P_{\mathrm{Distortion}}$ are the energy of the output signal, the noise floor, and the harmonic distortion. The results, corresponding to a bias voltage of $\pm$2.5 V, are shown in Fig. 9. An SNDR of 14 bits has been measured for both modulators, this performance loss (we expected a resolution of 16 bits) can be due to two main reasons: a reduced output swing of the operational transconductance amplifiers (OTAs), and to analog nonidealities related with switches. The same test has been repeated biasing the system at $\pm$1.65 V. The results for both tests are summarized in Table I.

TABLE I
Resolution of Both Modulators

Modulator	Bias Voltage	Resolution
Lineal	$\pm$ 2.5	> 14b
	$\pm$ 1.65	> 11b
Floating gate	$\pm$ 2.5	> 14b
	$\pm$ 1.65	> 10b

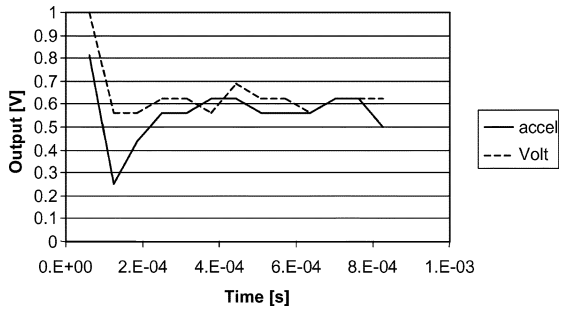

Fig. 10. Response of the interface (i) without accelerometer (dashed line) (ii) with accelerometer (continuous line).

Finally, we have connected an accelerometer to our interface and applied a unit step force equivalent to the electrostatic force generated by V_{ref}. This stimulus produces the output shown in Fig. 10.

To draw this plot, we have recorded the output of the modulator to calculate the mean value every 16 samples. We can see the behavior of the system when no acceleration is applied (dashed curve) and when an acceleration step is applied (continuous curve). In the first case the modulator goes to the steady point in 100 μs. This time, is necessary to discharge the reference capacitor. In the second case, the curve is delayed due to the accelerometer response. Taking into account that the system goes to a steady position when the perturbation is applied, we can conclude that the system is strictly stable [23] and confirm the results of the proposed stability analysis.

VI. Conclusion

The feasibility of a FB interface based on a second-order $\Delta\Sigma$ modulator for capacitive sensors has been analyzed in order to

delimit the requirements that the modulator has to fulfill to assure system stability for a given set of constraints, or, on the other hand, to determine the range of sensors that can be used with a given modulator.

The proposed solution has been implemented using a modulator architecture based on charge integrators. It has been shown that charge integrators can be designed using gate capacitors.

The proposal has been validated comparing the results from two $\Delta\Sigma$ interfaces one with linear capacitors and one with MOS capacitors successfully developed in a standard 0.7-μm single-poly CMOS technology.

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