Gallium–Indium–Zinc-Oxide-Based Thin-Film Transistors: Influence of the Source/Drain Material

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***Abstract*—During the last years, oxide semiconductors have shown that they will have a key role in the future of electronics. In fact, several research groups have already presented working devices with remarkable electrical and optical properties based on these materials, mainly thin-film transistors (TFTs). Most of these TFTs use indium–tin oxide (ITO) as the material for source/drain electrodes. This paper focuses on the investigation of different materials to replace ITO in inverted–staggered TFTs based on gallium–indium–zinc oxide (GIZO) semiconductor. The analyzed electrode materials were indium–zinc oxide, Ti, Al, Mo, and Ti/Au, with each of these materials used in two different kinds of devices: one was annealed after GIZO channel deposition but prior to source/drain deposition, and the other was annealed at the end of device production. The results show an improvement on the electrical properties when the annealing is performed at the end (for instance, with Ti/Au electrodes, mobility rises from 19 to 25 $cm^2/V \cdot s$, and turn-on voltage drops from 4 to 2 V). Using time-of-flight secondary ion mass spectrometry (TOF-SIMS), we could confirm that some diffusion exists in the source/drain electrodes/semiconductor interface, which is in close agreement with the obtained electrical properties. In addition to TOF-SIMS results for relevant elements, electrical characterization is presented for each kind of device, including the extraction of source/drain series resistances and TFT intrinsic parameters, such as μ_i (intrinsic mobility) and V_{Ti} (intrinsic threshold voltage).**

***Index Terms*—Amorphous oxide semiconductors, contact resistance, RF magnetron sputtering, thin-film transistors (TFTs).**

I. Introduction

THE THIN-FILM transistor (TFT) industry is still tightly connected to the silicon technology, and it will most likely remain that way during the next years. However, new research areas have been opened with the appearance of the first semiconductor oxide-based transistors in 1996 by Prins *et al.* [1]. At that time, little attention was given to the semiconductor material (Sb-doped SnO_2), but in 2003–2004, the "big boom" happened with the presentation of several oxide semiconductor TFTs based on ZnO [2]–[5] or ZnO compound materials [6] with remarkable electrical properties, which are comparable to or even better than amorphous silicon (a-Si) TFTs. Once these devices were reported, several ideas appeared concerning their application, with the main driving force related to the next generation of flexible and transparent devices processed at low temperatures, namely for display applications. In fact, from that time until today, several reports have been presented concerning (fully) transparent transistors with reduced processing temperatures and/or enhanced electrical properties in comparison with the first ZnO TFTs [7]–[9]. The key point that allowed this evolution was the exploitation of new multicomponent oxide semiconductors based on heavy-metal cations, e.g., zinc–tin oxide (ZTO) [8], indium–zinc oxide (IZO) [7], [9], [10], and gallium–indium–zinc oxide (GIZO) [11], which have excellent electrical properties in spite of their amorphous structure, something that is unusual for conventional covalent semiconductors [10]. As the field of oxide-based TFTs is still fairly recent, details about this technology need to be studied for a better understanding of the physics behind it, as it happens with the contact resistance issues, which are already widely explored in a-Si [12], [13] and organic-based TFTs [14]–[17]. The contact resistance is known to be a bottleneck factor on the performance of these devices, which is responsible for limiting, among other parameters, the transconductance (hence, the channel mobility), particularly in low-dimensional devices. Jackson *et al.* [18], using capacitance–voltage (C–V) measurements, reported that the Al/ZTO contact resistance was in the range of 100 kΩ, causing significant on-current degradation. This paper aims to provide an overview of the importance of the contact resistance on GIZO-based TFTs using different source/drain electrode materials (e.g., IZO, Ti, Al, Mo, and Ti/Au) and devices with different channel lengths.

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II. Experimental Details

The TFTs were produced using heavily doped ($N_A \approx 10^{17}$ cm^{-3}) p-type silicon substrates (2.5 × 2.5 cm) coated with 100-nm-thick thermally grown SiO_2, which acted as the gate dielectric. Si was simultaneously used as the substrate and the common gate of the devices. A Ti (15 nm)/Au (135 nm) film was deposited by electron beam (e-beam) evaporation on the backside of Si (after etching the backside SiO_2 with a buffered HF solution) to form the gate electrode.

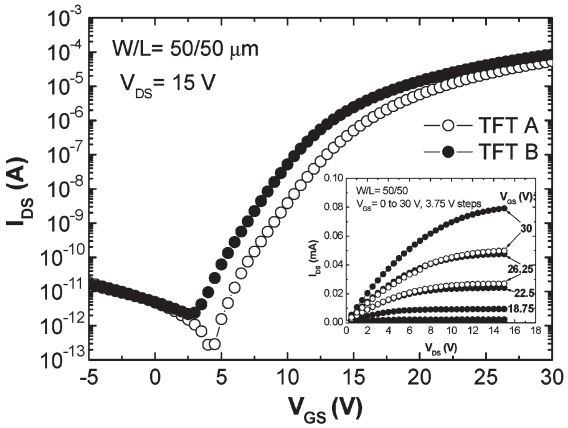

Fig. 1. Transfer characteristics of GIZO-based TFTs with Ti/Au source/drain electrodes annealed before (TFT A, open circles) and after (TFT B, closed circles) the deposition of Ti/Au. Inset shows the output characteristics of TFT B and TFT A (for high $V_{\rm GS}$), in which it is visible that for the same $V_{\rm GS}$ and $V_{\rm DS}$, $I_{\rm DS}$ is higher in TFT B. Devices with $W/L = 50/50\ \mu$m.

A 50-nm-thick GIZO layer (the semiconductor) was then deposited by RF magnetron sputtering at room temperature in a Pfeiffer Vacuum Classic 500 system. A 3-in-diameter ceramic target from LTS was used at 15 cm from the substrate, at a base pressure of 5×10^{-4} Pa, an oxygen partial pressure of 4×10^{-2} Pa, a processing pressure $(\mathrm{Ar} + \mathrm{O_2})$ of 7×10^{-1} Pa, and an RF power of 75 W. Different source/drain electrodes—Ti, Al, Mo, and Ti/Au, all 200 nm thick—were e-beam evaporated at a rate of 2 Å/s on top of GIZO to evaluate the influence of the various electrode materials on the electrical properties of the TFTs. In addition to these metals, IZO (200 nm) deposited by RF magnetron sputtering was also tested as a source/drain electrode material. The details concerning IZO can be found elsewhere [7]. Both the semiconductor and the source/drain layers were patterned by liftoff, and the produced transistors had a fixed width W of 50 μm, whereas the length L was changed between 50 and 5 μm. Two different kinds of transistors were produced with each source/drain material: one (TFT A) was annealed after GIZO but prior to source/drain deposition; the other (TFT B) was annealed at the end of device production. Annealing was performed in a Barnstead Thermolyne F21130 tubular furnace, with a constant flow of nitrogen, at 250 °C for 1 h.

III. Results and Discussion

Fig. 1 shows the transfer and output characteristics of GIZO-based TFTs with Ti/Au source/drain electrodes, which are annealed at two different processing stages—before (TFT A) and after (TFT B) source/drain deposition. The data reveal a general improvement on the electrical properties of device B, as traduced by an enhancement on the maximum $I_{\rm DS}$, i.e., $I_{\rm DS\,max}$ (0.08 against 0.05 mA), and the field-effect mobility $\mu_{\rm FE}$ (24.5 against 18.8 $\mathrm{cm^2/V \cdot s}$, as calculated by the transconductance with $V_{\rm DS} = 1$ V) and a slightly lower threshold voltage V_T (12.8 against 14.6 V). The on/off ratio remained essentially the same, i.e., around 6×10^7. This enhancement could be related to some changes in the interface between the source/drain and

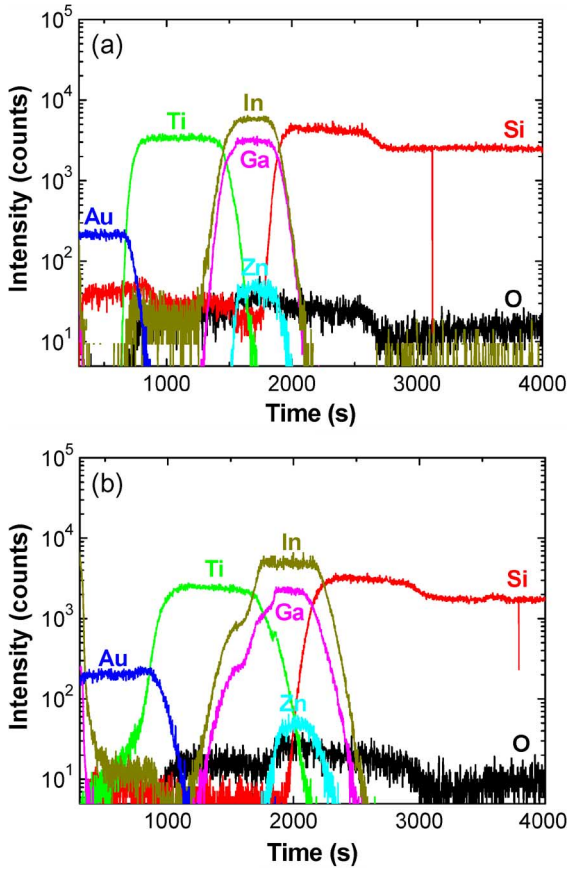

Fig. 2. Depth profile obtained by TOF-SIMS for the Ti/Au/GIZO/SiO_2 interfaces. (a) TFT A. (b) TFT B.

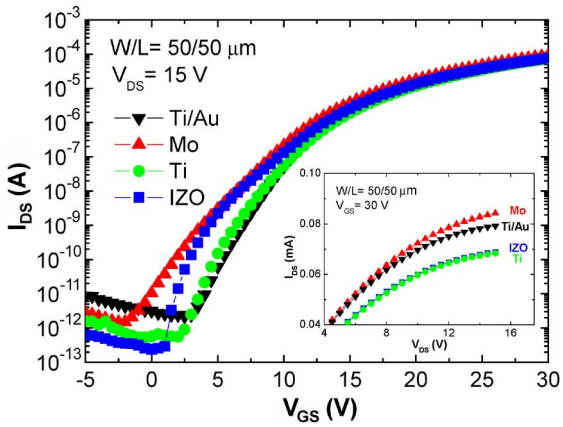

Fig. 3. Transfer characteristics of GIZO-based TFTs with different source/drain electrodes: IZO, Ti, Mo, and Ti/Au. Inset shows magnification for high $V_{\rm DS}$ of the output characteristics of the same devices. Devices with $W/L = 50/50\ \mu$m.

the semiconductor, such as a decrease of the barrier associated with the contact of materials with different workfunctions [19]. Indeed, by the results obtained using time-of-flight secondary ion mass spectrometry (TOF-SIMS) (Fig. 2), one can clearly see that TFT B data reveal a broader intersection between Au and Ti (the two metals that compose the source/drain electrodes and that obviously have an influence on the contact's electrical performance, where Ti is the adhesion layer) and Ti and GIZO than for TFT A. These broad intersections are related

TABLE I
COMPARISON OF THE ELECTRICAL PROPERTIES OF GIZO-BASED TFTS WITH DIFFERENT SOURCE/DRAIN ELECTRODES. DEVICES WITH $W/L = 50/50\ \mu$m

Source/Drain material	μ_{FE} (cm^2/Vs)	μ_{sat} (cm^2/Vs)	On/Off @ V_{DS}=15V	V_{on} @ V_{DS}=15V (V)	V_T @ V_{DS}=15V (V)
IZO	20.7	15.7	2.1×10^8	1.0	12.7
Ti	21.1	16.9	1.3×10^8	2.0	13.7
Mo	22.6	17.4	6.0×10^7	-2.0	12.5
Ti/Au	24.5	18.7	6.1×10^7	2.0	12.9

to the diffusion of the constituent materials and, thus, with the formation of transition regions between the electrodes and the semiconductor that should improve the electrical characteristics. This evolution of properties from device A to B is more drastic with Ti or Ti/Au electrodes and barely noticeable with Mo electrodes. From all the tested source/drain materials, IZO is the one that presents fewer changes from A to B, presumably because it should be very similar to GIZO in terms of structure. In fact, TOF-SIMS data of TFT A and TFT B with GIZO/IZO do not reveal any evidence of changes at the interfaces. The remaining analysis throughout this paper will be done for B devices.

A comparison between the various source/drain materials is shown in Fig. 3 for devices with $W/L = 50/50\ \mu$m. The data show some differences on the transfer characteristics, mainly the turn-on voltage $V_{\rm on}$, which is considerably more negative for Mo source/drain electrodes. This could be related to the results obtained by TOF-SIMS, where no clear evidence of interfacial layer was observed for Mo/GIZO. On the contrary, since an interfacial layer is formed when Ti (or Ti/Au) electrodes are used, presumably TiO_x (note that Ti has a small free energy of oxidation), this could be pushing $V_{\rm on}$ toward more positive values. We are currently working to experimentally clarify this point. Off-current variations can be attributed to device processing nonuniformity and measurement error, as revealed by the characterization of different devices processed under the same conditions in different runs.

The inset of Fig. 3 shows magnification of output characteristics, where it can be seen that Mo and Ti/Au allow higher $I_{\rm DS\,max}$ than IZO and Ti source/drain electrodes. This suggests that the first two contacts have a higher efficiency of injection than the last two contacts. Note that for high $V_{\rm DS}$ (when the TFT is getting closer to or is in the saturation mode), most of that voltage is dropped near the source (i.e., injecting contact) than near the drain [15], [17]. Thus, a highly efficient contact is necessary to attain good electrical properties. The previous statement obviously assumes that the contacts are associated with some resistances, as will be later explored.

The electrical properties of the TFTs with different source/drain electrodes are listed in Table I and are in agreement with the previous statements. In fact, mobility is higher for Ti/Au and Mo contacts, both in linear ($\mu_{\rm FE}$) and saturation ($\mu_{\rm sat}$) regimes. Note that $\mu_{\rm sat}$ is always lower than $\mu_{\rm FE}$, which can be attributed to the increased scattering effects in the channel due to the higher $V_{\rm DS}$ used to determine $\mu_{\rm sat}$. Concerning V_T and on/off ratio, no significant differences are found between all the electrodes, with the obtained values around 12.5–13.7 V and $6\times10^7 - 2\times10^8$, respectively.

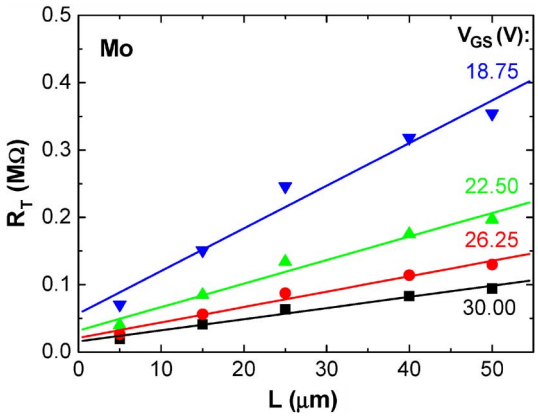

Fig. 4. Total TFT-ON resistance as a function of L and $V_{\rm GS}$ for a GIZO-based TFT with Mo source/drain electrodes. The experimental points are determined by the reciprocal of the slope (i.e., ON resistance) of the output characteristics for $V_{\rm DS} < 1.5$ V.

To evaluate the performance of different materials, the contact resistance and intrinsic semiconductor parameters were studied. For a low $V_{\rm DS}$, the total TFT-ON resistance R_T can be written as [20]

$$R_T = \frac{V_{\rm DS}}{I_{\rm DS}} = r_{\rm ch}L + R_S + R_D \tag{1}$$

where $r_{\rm ch}$ is the channel resistance per channel-length unit, and R_S and R_D are the series resistances associated with the source and drain, respectively. Using the basic transistor equation from the gradual channel approximation, $r_{\rm ch}$ is given by [20]

$$r_{\rm ch} = \frac{L}{\mu_i C_{\rm ox} W (V_{\rm GS} - V_{\rm Ti})} \tag{2}$$

where μ_i and $V_{\rm Ti}$ are the intrinsic semiconductor mobility and threshold voltage, respectively, representing the conduction channel without the influence of the contact series resistance. The determination of these parameters involves the determination and plotting of R_T (at low $V_{\rm DS}$, i.e., in linear regime) for different $V_{\rm GS}$ and L, then fitting the experimental values with linear curves for each $V_{\rm GS}$ (Fig. 4). The intercept with the y-axis of each fitting gives $R_S + R_D$, whereas $r_{\rm ch}$ is given by the slope, as evidenced by (1). Plotting the reciprocal of $r_{\rm ch}$ as a function of $V_{\rm GS}$ and fitting the results with a linear curve, μ_i (slope) and $V_{\rm Ti}$ (x-axis interception) can be obtained according to (2).

The obtained intrinsic parameters are shown in Fig. 5, together with the evolution of $\mu_{\rm FE}$ and V_T with L. Concerning

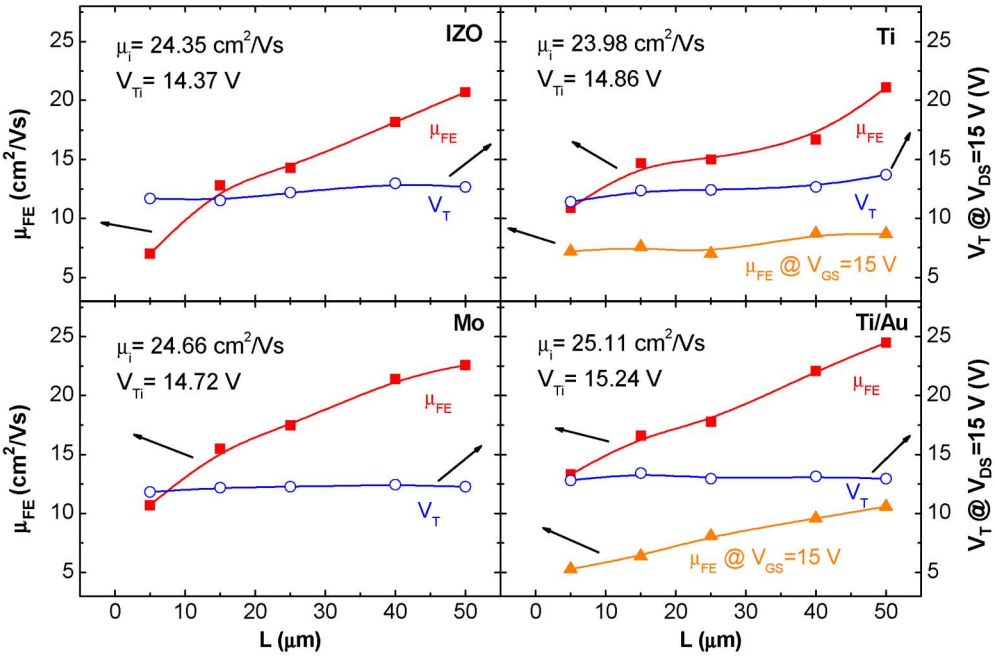

Fig. 5. Evolution of peak $\mu_{\rm FE}$ (closed boxes) and V_T (open circles) with L for GIZO-based TFTs with different source/drain electrodes: IZO, Ti, Mo, and Ti/Au. For Ti and Ti/Au, $\mu_{\rm FE}$ versus L is also presented for $\mu_{\rm FE}$ determined at $V_{\rm GS} = 15$ V (closed triangles). The intrinsic parameters μ_i and $V_{\rm Ti}$ are also presented for each device.

the intrinsic parameters, namely μ_i and $V_{\rm Ti}$, no considerable changes were verified among the tested material, which is an expectable result since the model takes into account that part of the applied $V_{\rm GS}$ is dropped by the source/drain contact resistances.

In all the devices, $\mu_{\rm FE}$ follows the same trend as L, i.e., it decreases for small channel lengths. Two aspects are worth noticing here. 1) The μ_i values match quite well with the $\mu_{\rm FE}$ values of devices with a long channel (50 μm); this means that, in this case, R_S and R_D should not be of significant influence. 2) As L decreases, the relative influence of R_S and R_D in R_T increases (R_S and R_D are independent of L, but the product $r_{\rm ch} \times L$ decreases); thus, a larger voltage is dropped at the contact resistances for smaller L, thus lowering $\mu_{\rm FE}$ [17]. In particular, this means that the real voltages (both $V_{\rm DS}$ and $V_{\rm GS}$) applied inside the device, after passing the electrodes, are diminished as L decreases. This relative effect of the resistances is clearly seen in Fig. 6, where both $R_C = R_S + R_D$ and $r_{\rm ch} \times L$ for various L are plotted as a function of $V_{\rm GS}$.

For all the materials, both $r_{\rm ch} \times L$ and R_C are $V_{\rm GS}$ dependent, i.e., they decrease for larger $V_{\rm GS}$. This can be justified by the increase of the carrier concentration as $V_{\rm GS}$ increases, both in the channel (the field effect phenomenon) and outside the channel defined by the lithographic mask (i.e., outside the space defined by L), since source/drain to gate overlaps exist [13], [14]. In the present case, since the gate electrode covers all the substrate, this overlap is maximized.

As shown in Fig. 6, as L increases, the contribution of R_C to R_T decreases, agreeing quite well with the data depicted in Fig. 5. For instance, if long and short devices ($L = 50$ and 5 μm) are considered, different evolutions of $\mu_{\rm FE}$ are observed:

For $L = 50$ μm, since the R_C contribution to R_T is negligible throughout the range of the studied $V_{\rm GS}$, $\mu_{\rm FE}$ will mostly depend on $r_{\rm ch}$, which is low for devices where the source/drain electrodes are based on Ti/Au and Mo and high for those based on IZO and Ti. Thus, $\mu_{\rm FE}$ increases in the following order of the materials used for the source/drain electrodes, i.e., IZO, Ti, Mo, and Ti/Au, as shown in Table I. Now, even if one does not calculate the peak value of $\mu_{\rm FE}$ (note that until now, only this value was presented, with the peak located around $V_{\rm GS} = 25 - 30$ V) but rather $\mu_{\rm FE}$ for a smaller $V_{\rm GS}$, e.g., 15 V, where R_C is higher, the order presented for $\mu_{\rm FE}$ is still preserved since $r_{\rm ch}$ continues to be much higher than R_C.

For $L = 5$ μm, R_C is comparable to or even higher than $r_{\rm ch} \times L$ throughout the $V_{\rm GS}$ range; thus, both R_C and $r_{\rm ch} \times L$ are significant to R_T. For $V_{\rm GS} = 30$ V, the $\mu_{\rm FE}$ order for the different materials previously listed remains essentially the same. However, for $\mu_{\rm FE}$ determined at $V_{\rm GS} = 15$ V, the situation is quite different since R_C is dominant in R_T for all the materials except Ti. Thus, in this case, $\mu_{\rm FE}$ increases in another order, i.e., Ti/Au, IZO, Mo, and Ti.

Taking into account the aforementioned conditions, we can now go back to Fig. 5 and plot the evolution of $\mu_{\rm FE}$ with L at $V_{\rm GS} = 15$ V. The results show, as expected, only a very small variation of $\mu_{\rm FE}$ with L for Ti, whereas for Ti/Au, a clear increase of $\mu_{\rm FE}$ with L is observed. This reinforces the idea that R_C has a strong effect on the electrical properties of the TFTs.

Finally, it remains unclear what happens when Al is used for the source/drain electrode. In this case, we always noticed severe current crowding in the output characteristics at low $V_{\rm DS}$, which is independent of when the annealing treatment is performed (before or after depositing the electrodes). Thus, it seems that a considerable barrier is formed between Al and GIZO, which makes it impossible to do any reliable characterization in the linear regime.

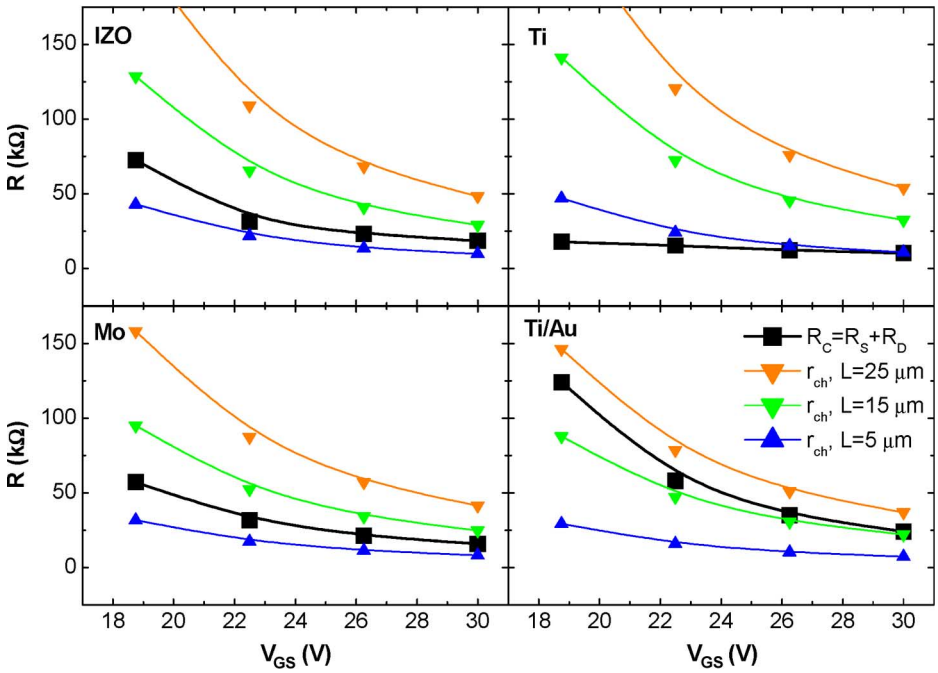

Fig. 6. Evolution of R_C (contact resistance) and $r_{\rm ch} \times L$ (channel resistance) for different values of L (5, 15, and 25 μm) with $V_{\rm GS}$ for GIZO-based TFTs with different source/drain electrodes: IZO, Ti, Mo, and Ti/Au

IV. Conclusion

The role of the contact resistance was analyzed in GIZO-based TFTs with different source/drain electrodes. The influence of the annealing step, before or after the deposition of source/drain electrodes, was studied and led to the conclusion that devices with improved electrical properties are generally obtained for the last case. Concerning the different source/drain materials, Ti/Au led to the highest $\mu_{\rm FE}$, whereas V_T and on/off ratio were similar for all the tested materials. Evolution of $\mu_{\rm FE}$ and V_T with L revealed no significant variation of V_T, but a pronounced decrease of $\mu_{\rm FE}$ for lower L was observed, which was ascribed to the higher relative influence of the contact resistance on the total resistance of short-channel devices. For high $V_{\rm GS}$, when R_C started to saturate at a minimum value, R_C was found to be in the range of 10 (Ti) to 20 (Ti/Au) kΩ, with these values around one order of magnitude lower than the 100 kΩ presented by Jackson *et al.* for ZTO-based TFTs with Al contacts. A more detailed analysis of the contact resistance issues and their role in all device performances is underway by the present working team, which aims to improve the overall device performance, including the transport mechanism that takes place between the source/drain and the channel region.

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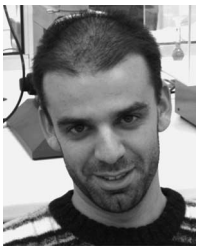

Pedro Barquinha was born in Lisbon, Portugal, on May 9, 1980. He received the Eng. degree in materials science in 2004 from the New University of Lisbon, Caparica, Portugal, where is currently working toward the Ph.D. degree under the supervision of Prof. E. Fortunato. His thesis was focused on the study of zinc oxide and its application as a semiconductor in fully transparent TFTs.

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Rodrigo Martins was born in 1951. He received the M.Sc. degree in amorphous semiconductor technologies from Dundee University, Dundee, U.K., in 1977 and the Ph.D. degree in semiconductors and the Aggregation (teaching certificate) in microelectronics from the New University of Lisbon, Caparica, Portugal, in 1982 and 1988, respectively.

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Prof. Morante is a member of international committees and editorial teams of journals and has been a Guest Editor of many special issues. He has been awarded the Narcís Monturiol of the Generalitat of Catalunya and the Senior Research Distinction Award from the Generalitat of Catalunya.

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Prof. Fortunato has been an Associate Editor of *Physica Status Solidi (Rapid Research Letters)* since November 2006 (Wiley). She was the recipient of the Scientific Excellence Award from the Portuguese Science Foundation (FCT-MCTES) in 2005 and the Gold Medal Award from the Municipality of Almada in 2007.