

# Kelvin probe measurements of microcrystalline silicon on a nanometer scale using SFM

A. Breymesser<sup>a,\*</sup>, V. Schlosser<sup>a</sup>, D. Peiró<sup>b</sup>, C. Voz<sup>b</sup>, J. Bertomeu<sup>b</sup>, J. Andreu<sup>b</sup>, J. Summhammer<sup>c</sup>

<sup>a</sup>Institute for Material Physics, University of Vienna, Strudlhofgasse 4, A-1090 Vienna, Austria

<sup>b</sup>Departament de Física Aplicada i Òptica, Universitat de Barcelona, Av. Diagonal 647, E-08028 Barcelona, Spain

<sup>c</sup>Atom Institute of the Austrian Universities, Stadionallee 2, A-1020 Vienna, Austria

\*Corresponding author. Tel.: +43-(0)1-586 34 08-27; fax: +43-(0)1-586 34 08-13; e-mail: e8727675@student.tuwien.ac.at

## Abstract:

Work function measurements on cross sectioned microcrystalline pin silicon solar cells deposited by Hot-Wire CVD are presented. The experiment is realized by combining a modified Kelvin probe experiment and a scanning force microscope. The measured surface potential revealed that the built-in electric drift field is weak in the middle of the compensated intrinsic layer. A graded donor distribution and a constant boron compensation have to be assumed within the intrinsic layer in order to obtain coincidence of the measurements and simulations. The microcrystalline p-silicon layer and the n-type transparent conducting oxide form a reverse polarized diode in series with the pin diode.

Keywords: Microcrystalline silicon; Kelvin force microscopy; Nanopotentiometry; Thin film solar cells; Surface potential.

## 1. Introduction

The combination of a modified Kelvin probe experiment with a scanning force microscope (SFM) opens the door to work function measurements with submicron resolution (nanopotentiometry,

scanning Kelvin probe microscopy). The application of nanopotentiometry on semiconductors is of special interest because the position of the Fermi level depends on doping levels, space charge regions and free carrier concentrations [1].

Nanopotentiometric measurements were carried out on  $\mu\text{c-Si}$  solar cells. A pin structure was chosen for the cells due to the low diffusion lengths of electrons and holes in  $\mu\text{c-Si}$ . The collection of photogenerated charge carriers is assisted by the built-in electric drift field in the intrinsic layer. The quality of the intrinsic layer is a critical point in order to obtain reasonable electric field strengths over the entire layer. On the one hand the usefulness of work function measurements of thin film solar cell structures for characterization purposes should be proved. On the other hand cross sections of actual  $\mu\text{c-Si}$  thin film solar cells were investigated in order to suggest improvements for the deposition process.

## 2. Experimental

The basis of the experiment is a commercially available Topometrix Explorer 2000 atomic force microscope (AFM) operated in noncontact mode and a modified Kelvin experiment added to the AFM. The AFM tip and the semiconducting sample form a kind of capacitor. Applying an AC voltage with a frequency  $\omega$  (about 50kHz) to this capacitor it oscillates with the excitation frequency when there is a superimposed DC voltage coming from contact potential and externally applied voltages. A lock-in amplifier was used to determine the cantilever oscillation amplitude at  $\omega$ . Regulating the externally applied DC voltage to the same value as the contact potential with opposite sign the oscillation at  $\omega$  vanishes [1]. The compensating DC voltage was generated by a proportional-integral regulator. Nanopotentiometry and noncontact topography were measured simultaneously in ambient air. Commercially available highly doped diamond coated silicon tips with a resonance frequency of 75kHz, a force constant of 2.8N/m and a typical tip radius of about 100nm (nanoroughness 10nm) were used. The nanopotentiometric measurements were always carried out off the fundamental resonance since it was needed for the topography measurement. The Kelvin excitation AC voltage amplitude was chosen in the range of volts.

Ga doped ZnO deposited on glass with a thickness of about 400nm was used as a conducting substrate for the diodes. The diode structures were deposited by Hot–Wire CVD (HWCVD). Deposition temperatures were 175°C for the p–layer (100nm) which was the first layer on the transparent conducting oxide (TCO) and 215°C for the active i–layer (800nm) and the n–layer (50nm). The thicknesses were derived from deposition parameters. All layers were obtained with 95% hydrogen dilution of silane and a process pressure of  $7 \cdot 10^{-3}$  mbar. The doped layers were prepared by adding diborane or phosphine to the silane–hydrogen gas mixture. From C–V measurements on rectifying ZnO/undoped intrinsic  $\mu$ c–Si Schottky structures a donor trap density of about  $10^{17} \text{cm}^{-3}$  was estimated which was primarily attributed to oxygen contamination. Therefore the intrinsic layer was doped by a highly reduced flow of diborane to compensate the unwanted n–type character. The positive effect of compensation on solar cell parameters was proved by a better quantum efficiency and higher short circuit currents [2]. The solar cells had an open circuit voltage of about 0.3V and a short circuit current of  $8 \text{mA/cm}^2$  ( $100 \text{mW/cm}^2$  illumination intensity). For nanopotentiometry diode cross sections were prepared by cutting, grinding and polishing. In order to prevent damage of the regions of interest during preparation two diodes were glued together with their metal contacted n–doped layers. Due to the preparation process a homogeneous distribution of surface states on the silicon surface had to be expected. No surface passivation could be applied because chemical or thermal treatment would alter the silicon thin films. So no quantitative but only qualitative information could be derived from surface potential measurement because the surface states influence the position of the Fermi level (Fermi level pinning).

### 3. Results and discussion

The layer structure can be clearly seen in the twodimensional surface potential scan (right part of fig. 1). The contrast can be attributed to the different dopants and space charge regions. In the corresponding topography image (left part of fig. 1) only the transitions from glass to TCO and from n–type Si to the glue are visible due to different abrasion behaviour of the materials during preparation. For the surface potential line scan graph of fig. 2 a single line measurement was averaged 50 times. At the layer transitions there is a big change in potential whereas in the middle

of the intrinsic layer the potential change is only small which is a hint on poor compensation of charged defects. The electric field plot in the same graph obtained by derivation of the surface potential signal shows the insufficient compensation more clearly. The field strength is big at the layer transitions due to the space charge regions. In the middle of the intrinsic layer it drops to low values instead of remaining constant at a high field strength as intended in the intrinsic region. Mainly at the layer transitions drift field assisted charge carrier separation can be expected. This fact seems to be partially responsible for the low short circuit currents due to insufficient collection of charge carriers. Quantum efficiency measurements were carried out with front and backside illumination (fig. 3). The curves obtained with front side illumination also hint on the existence of two different charge separating regions. The quantum efficiency curve can be modelled as a sum of two curves attributed to the p/i and the i/n transition respectively. Charge carriers generated in the middle of the intrinsic layer are not sufficiently collected due to the lack of a high drift field and a small diffusion length of electrons and holes. In fig. 4 the effective charge concentration obtained by twofold derivation of the measured surface potential can be seen.

DLTS measurements were carried out to obtain knowledge on the kind of defects affecting the electric field distribution in the intrinsic region. Frequency dependent capacitance–voltage and conductance–voltage measurements confirmed that the DLTS measurements provided information on defects in the crystalline phase [3]. DLTS measurements on undoped  $\mu\text{c-Si/ZnO}$  rectifying Schottky diode structures revealed three easily resolvable donors with activation energies of 0.027eV, 0.185eV potentially induced by interstitial  $\text{Cu}^+$  and 0.336eV which may be attributed to tungsten from the hot filament. One acceptor with an activation energy of 0.104eV could be resolved. DLTS on pin diodes revealed three more shallow donor levels with activation energies lower than 0.140eV attributed to oxygen [3]. Despite the presence of a noncrystalline phase usually causing defect induced band tails as observed by optical absorption measurements distinct defect levels could be measured by DLTS typical for crystalline material.

From fig. 4 and simulations using the onedimensional semiconductor device simulation program PC1D a charged defect distribution shown in fig. 5 is proposed (compare with fig. 4). In the intrinsic layer a graded defect distribution and a constant boron compensation have to be assumed in

order to obtain the shape of the surface potential line scan by simulations. The gradation of the defect distribution may result from incorporation of residual impurities in the deposition chamber or outdiffusion of the ZnO layer. A defect distribution known from amorphous silicon (dangling bonds, band tails) would yield a similar shape of the surface potential. But due to the relatively low measurement frequency the crystalline phase plays the dominant role in nanopotentiometry [3]. At the transition from the p-doped  $\mu\text{-Si}$  layer to the n-type ZnO:Ga a reverse polarized diode compared to the pin diode can be deduced from fig. 2. This is possibly responsible for the low open circuit voltages of the solar cells.

#### 4. Conclusions

From nanopotentiometric measurements and simulations it can be derived that there is a graded donor like defect distribution in conjunction with an intentionally introduced constant compensating boron concentration in the intrinsic silicon layer of the investigated  $\mu\text{-Si}$  pin diodes. The effective charge distribution yields only a weak built-in electric drift field in the middle of the intrinsic layer resulting in reduced drift field assisted collection of charge carriers. Besides defect control it is suggested to introduce rather a graded than a constant boron concentration in the intrinsic layer during deposition in order to obtain a compensation profile which better fits the actual unintended donor distribution. To prevent the problems with the reverse polarized p-Si/n-TCO diode experiments on reverse stacking of the doped layers will be done. Future investigations will be carried out with illumination and diode bias voltages in order to extend the results to photovoltaic generator conditions [4, 5].

## References

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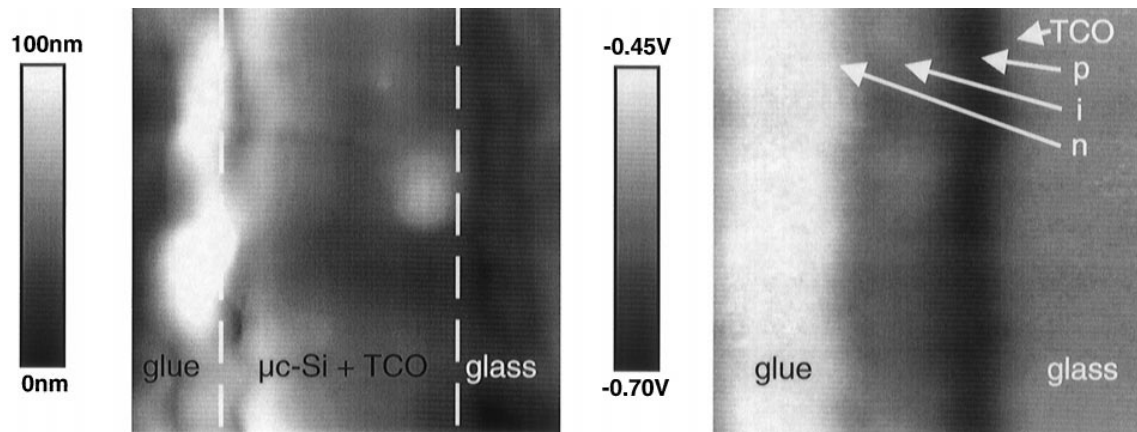


Fig. 1. Topography (left) and corresponding surface potential scan (right) of a cross-sectioned  $\mu\text{c-Si}$  pin diode. Scan size is  $3.5\ \mu\text{m}\times 3.5\ \mu\text{m}$ .

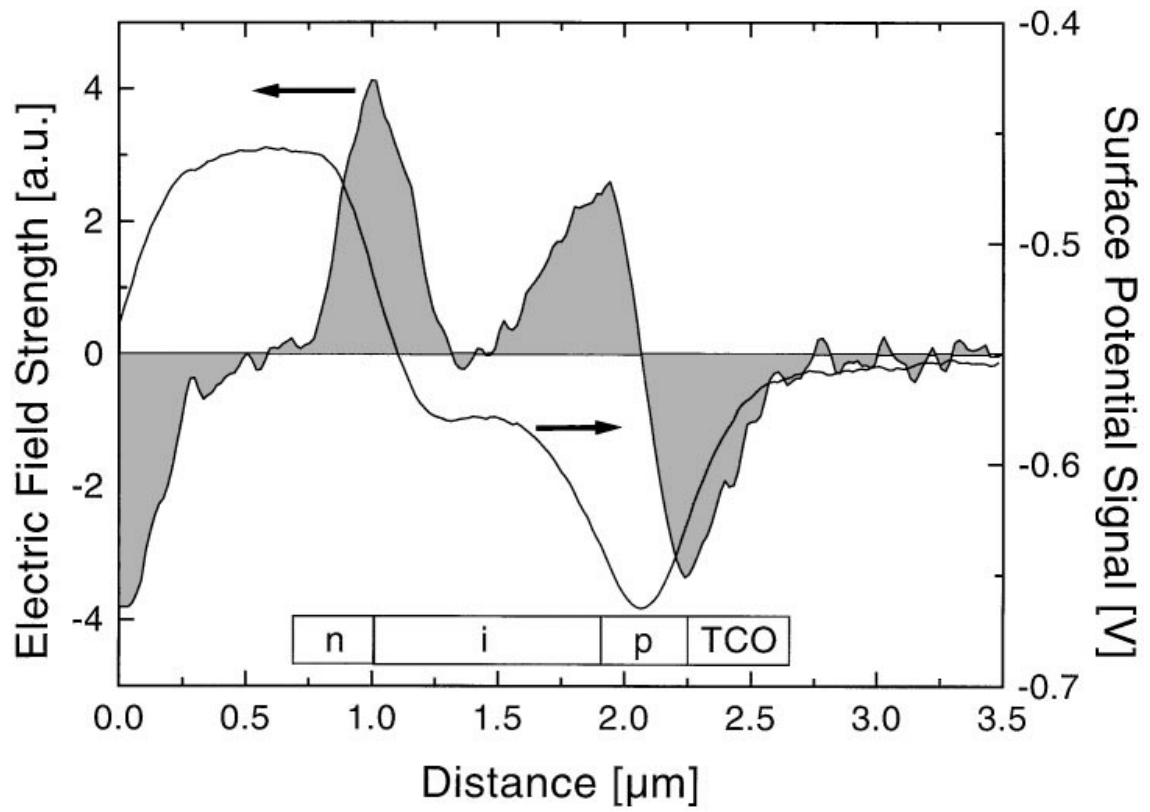


Fig. 2. Averaged surface potential line scan and calculated electric field strength (average of 50 lines) of the sample from Fig. 1.



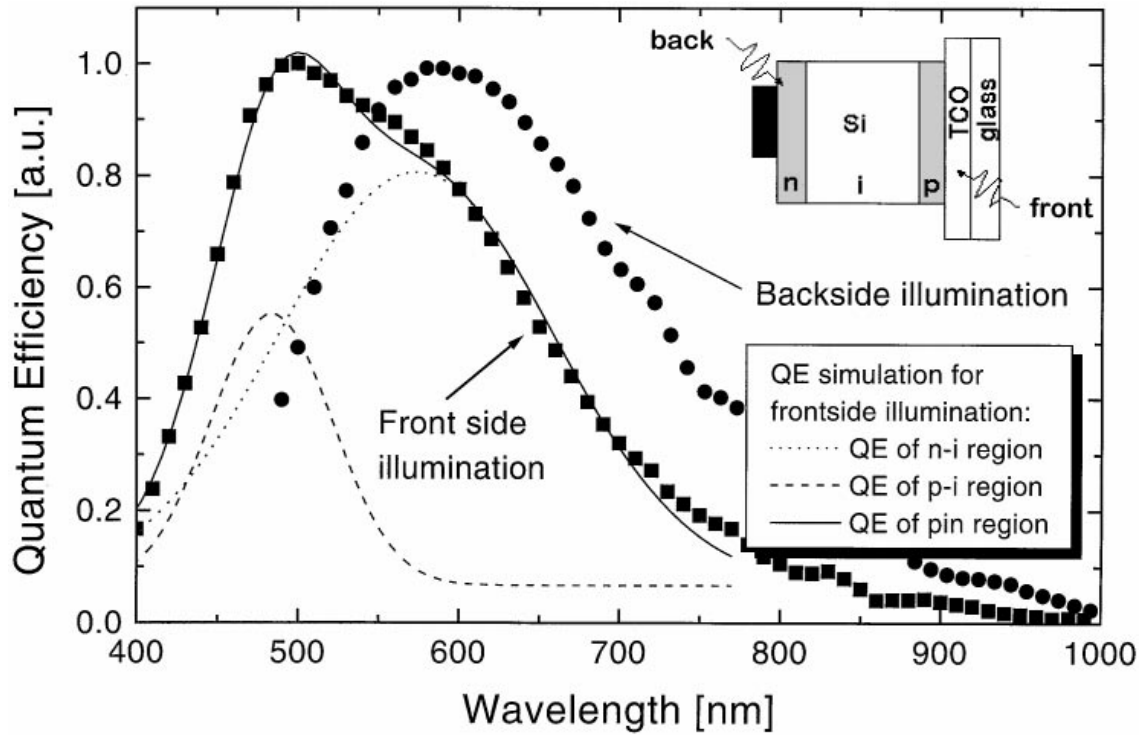


Fig. 3. Measured quantum efficiency with front- and back-side illumination of the sample from Fig. 1. The front-side illuminated quantum efficiency can be modelled as the sum of two contributions indicated by the dashed curves.

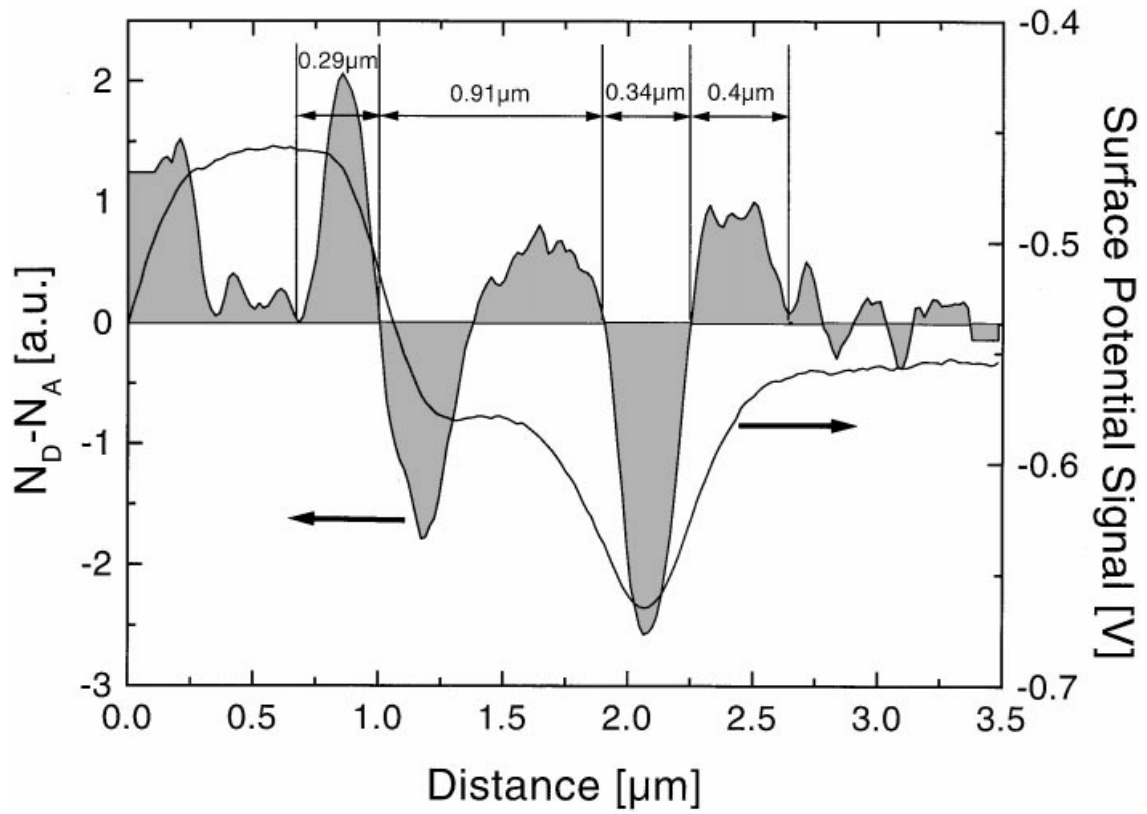


Fig. 4. Averaged surface potential line scan and calculated charged defect distribution (average of 50 lines) of the sample from Fig. 1.

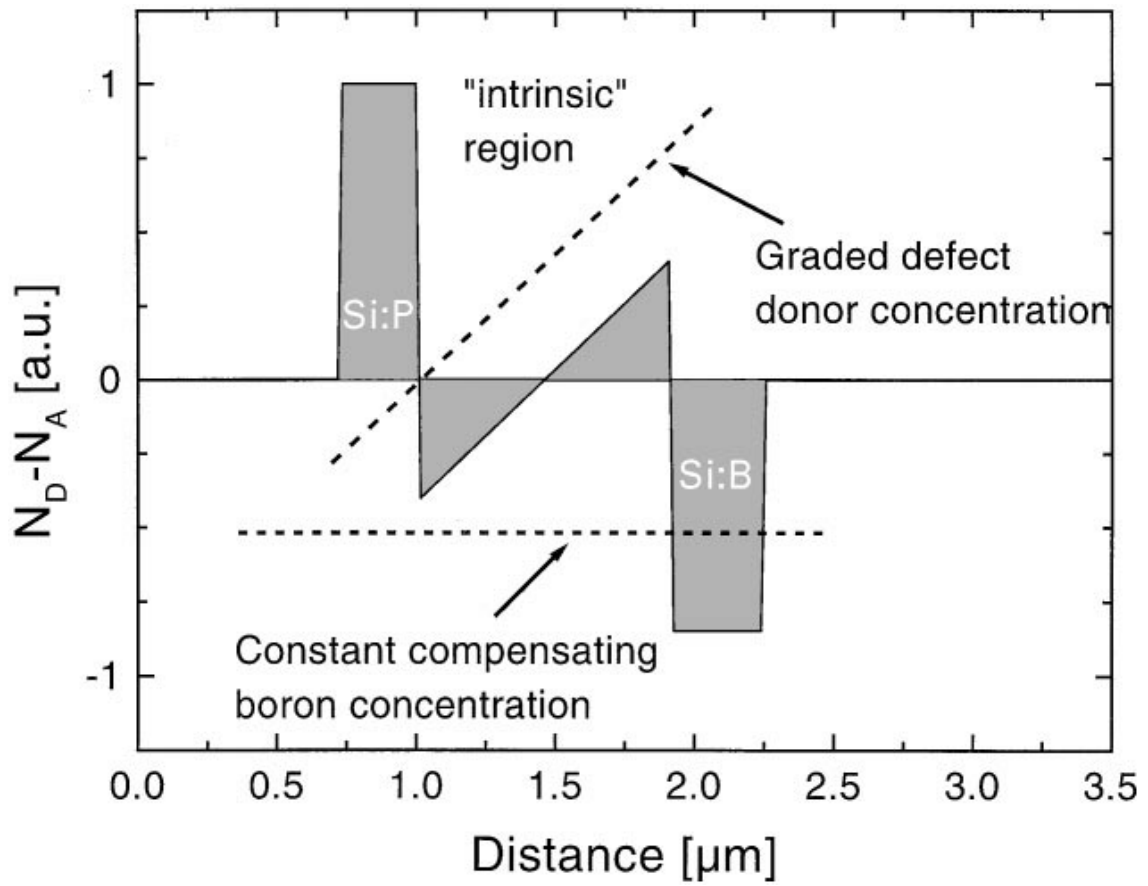


Fig. 5. Proposed charged defect distribution derived from the comparison of PC1D simulations and measurements (compare with Fig. 4).